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الجمهورية الجزائرية الديمقراطية الشعبية
Ministry of Higher Education and Scientific Research
وزارة التعليم العالي و البحث العلمي

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Department of Electrical Engineering
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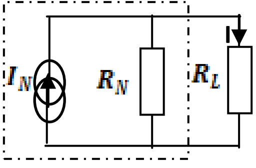
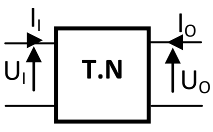
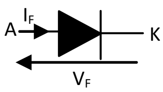
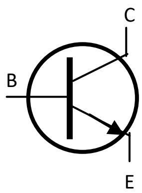
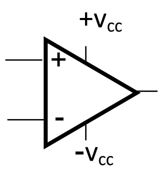
Fundamental Electronics 01











Presented by: Dr. Chabachi Salem

Intended for 2nd-Year Undergraduate Students

Field: Science and Technology (ST)

Specialty: *Electronics / Electrotechnics / Automatics (L2 – S3)*

Academic Year: 2025/2026

Acknowledgements

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Abbreviations

AC : Alternating Current

AP-OMP :OPerationl AMPlifiers

BJT : Bipolar Junction Transistor

CDR : Current Divider Rule

DC : Direct current

KCL : Kirchoff's Current Law

KVL : Kirchoff's Voltage Law

MPTT: Maximum Power Transfer Theorem

VDR : Voltage Divider Rule

Liste of figures

Liste of Tables

CONTENTS

Foreword

This course is designed to provide second-year undergraduate students in the field of *Science and Technology*, *specialty* ***Electronics / Electrotechnics / Automatics***, with the fundamental knowledge and theoretical as well as practical concepts necessary to understand the basic principles of electronics and their various applications. **It follows the official syllabus for the module "Fundamental Electronics 1".**

This course, titled ***Fundamental Electronics 1***, enables students to perform calculations, analyze, and interpret electronic circuits. It also helps them understand the properties, electrical models, and characteristics of electronic components such as diodes, bipolar transistors, and operational amplifiers.

The course is divided into five chapters:

1. **The first chapter** presents general concepts related to the application of Ohm's and Kirchhoff's laws, as well as methods for analyzing DC circuits (including the theorems of Norton, Thévenin, Superposition, Kennelly, Millman, and Maximum Power Transfer).
2. **The second chapter** covers passive two-port networks (quadripoles) in detail. Topics include: matrix representations of two-port networks, combinations of quadripoles, relationships between parameters, and the quantities characterizing a quadripole's behavior in a circuit, such as input and output impedance, and current and voltage gain. This chapter also includes frequency analysis of RC, CR, and RLC filters (transfer functions and Bode plots), to highlight the frequency-filtering properties of these electrical circuits.
3. **The third chapter** provides a review of semiconductors as an introduction to PN junctions and junction diodes. It also studies circuits based on diodes, such as half-wave and full-wave rectifiers, along with different types of diodes (Zener diode, Schottky diode, Varicap diode, light-emitting diodes, and photodiodes).
4. **The fourth chapter** is dedicated to the static and dynamic operation of bipolar junction transistors (BJTs), including various configurations such as common-emitter, common-base, and common-collector setups, as well as multi-stage amplifiers.
5. **The final chapter** addresses the operation of one of the most widely used and popular integrated circuits: the operational amplifier. It covers different types of configurations, particularly linear applications such as adders, subtractors, integrators, and differentiators

Chapter 01

DC NETWORK THEOREMS

1 DC NETWORK THEOREMS

Learning Objectives :

By studying the information and completing the exercises in this chapter, the student will be able to:

- Understand the fundamental laws used in DC circuit analysis.
- Explain the structure and behavior of electric circuits and networks.
- Understand the voltage–current relationship of resistors according to Ohm's Law.
- Identify and understand the basic elements of electrical circuits, including nodes, loops, and branches.
- Calculate equivalent resistances in series and parallel configurations.
- Apply Kirchhoff's Laws (KCL & KVL) to analyze electrical circuits.
- Use the Voltage Divider Rule (VDR) to determine voltages in series circuits.
- Use the Current Divider Rule (CDR) to determine currents in parallel circuits.
- Apply the Superposition Theorem to analyze circuits with multiple independent sources.
- Apply Thevenin's and Norton's theorems to simplify complex electrical networks.
- Convert between Thevenin and Norton equivalent circuits and understand their relationship.
- Use source transformation techniques in circuit simplification.
- Understand the concept and significance of Millman's Theorem in circuit analysis.
- Apply Kennelly (Δ–Y / Y–Δ) transformation for simplifying circuit networks.
- Understand and apply the Maximum Power Transfer Theorem to determine optimal load conditions.

1.1 Definitions and Terminologies

- **Electric Network** A combination of various electric elements, connected in any manner whatsoever, is called an electric network.
- **Parameters**. The various elements of an electric circuit are called its parameters like resistance, inductance and capacitance. These parameters may be lumped or distributed.
- **Node** A connection point of several circuit elements is termed as a *node*. For instance, A, B, C, and D are foure nodes in the electric network of Figure 1-1.
- **Loop.** It is a close path in a circuit in which no element or node is epcountered more than once.
- **Branch** is that part of a network which lies between two juncions.
  AB, AD, BD,DC and BC are six branches in the network of Figure 1-1.

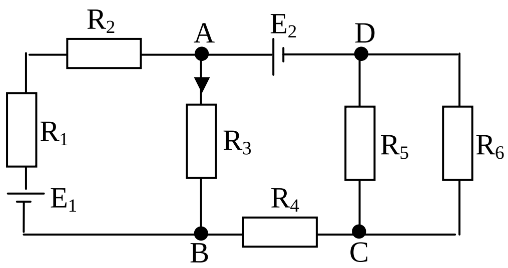
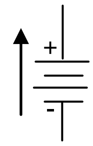
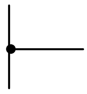
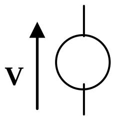
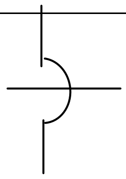
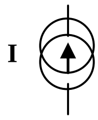
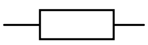
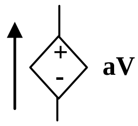
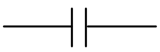
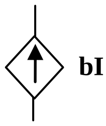
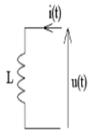
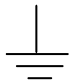
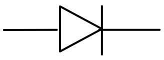
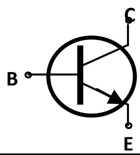
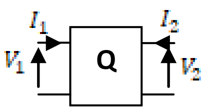
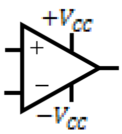
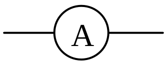
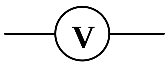


Figure 1-1: Electric Network

1.2 Circuit symbol

A circuit symbol is a simple picture that is used to represent an electrical component when drawing a circuit diagram (Table1-2).

Table 1-1 : Circuit symbol

Schematic	Circuit Element	Schematic	Circuit Element
	Wire		Battrey
	Junctions		Voltage source
	Wires crossing		Current source
	Resistor		Dependent voltage source
	Capacitor		Dependent current source
	Inductor		Ground
	Diode		Transistor
	Two porte Electrique		Operatienl opmlifier
	Ampermetre		Voltmeter

1.3 Electric current

Electric current is the time rate of change of charge, measured in amperes (A).

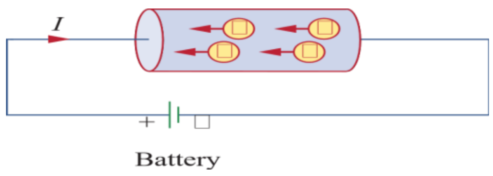


Figure 1-2: Electric current due to flow of electronic charge in a conductor

Mathematically, the relationship between current i, charge q, and time t is

$$i = \frac{dq}{dt} \tag{1.1}$$

where:

i= current

q= total charge moved (in coulombs)

t = time taken (in seconds)

Two common types of current:

1.3.1 Alternating current (AC):

An alternating current (AC) is a current that varies with time (sinusoidally Figure 1-3.a)

1.3.2 Direct current (DC):

A direct current (DC) is a current that remains constant with time Figure 1-3.b

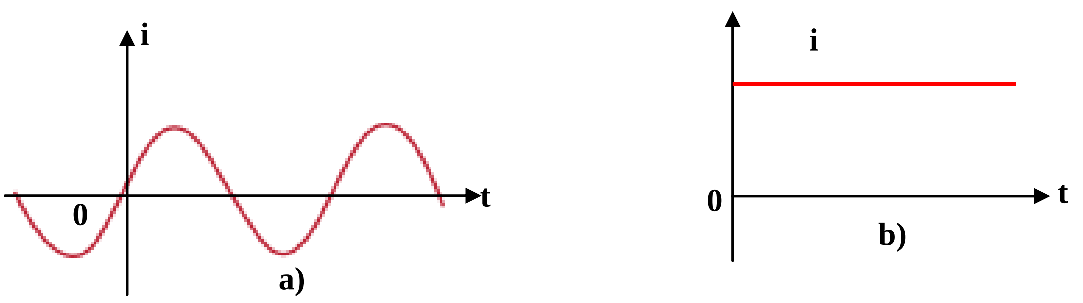


Figure 1-3 : Two common types of current: (a) alternating current (AC). (b) direct current (DC)

1.4 Voltage (or potential difference)

Voltage (or potential difference) between points A and B, is defined to be the change in potential energy of a charge q moved from A to B, divided by the charge, measured in volts (V).

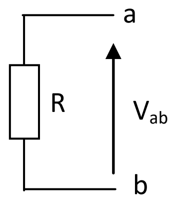


Figure 1-4: Polarity of voltage

mathematically,

$$v_{ab} = \frac{dw}{dq} \tag{1.2}$$

v_{ab}: potential difference between points a and b

w: work done to move charge q

q : amount of charge moved

1.5 Passive and active elements

- ✓ **Active elements** is one which contains one or more than one source of e.m.f. exemple : voltage and curent sources.
- ✓ **Passif elements**: is one which contains no source of e.m.f in it example : résistances, capacité and bobine.

1.5.1 Passif elements

1.5.1.1 What is resistor?

The Resistors is a passive electrical component with the primary function to limit the amount of current or to produce a desired drop in voltage.

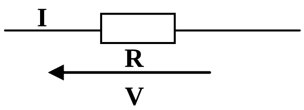


Figure 1-5: Resistor

Ohm's Law

Ohm's law establishes a direct proportional relationship between the voltage across a resistor and the current through it:

$$V = RI \tag{1.3}$$

1.5.1.2 Resistor in series

Consider figure 1-6 with one voltage source and two resistors connected in series to form a single mesh with current *I*.

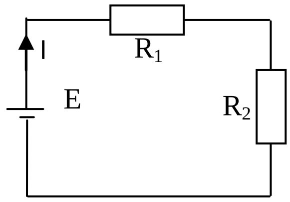


Figure 1-6 : Series combination of two resistors

Applying KVL, we get:

$$E = U_1 + U_2 = R_1 I + R_2 I = (R_1 + R_2) I = R_{eq} I \tag{1.4}$$

$$R_{eq} = R_1 + R_2 \tag{1.5}$$

The equivalent resistance of any number of resistors connected in series is the sum of the individual resistances.

$$R_{eq} = \sum_{i=1}^{i=N} R_i \tag{1.6}$$

For N resistors in series then

1.5.1.3 Resistors in Parallel

Consider figure 1-7 with a single current source and two resistors connected in parallel. All parallel circuit elements have the same voltage, *V* across them i.e. $V_1 = V_2 = E$

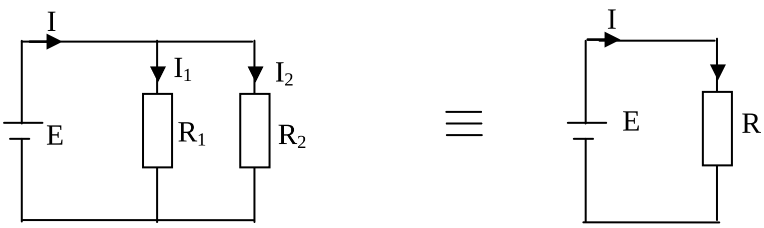


Figure 1-7 : Parallel connection of resistors

Applying KCL, we get:

$$I = I_1 + I_2 = \frac{E}{R_1} + \frac{E}{R_2} = E\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{1.7}$$

$$\Rightarrow \frac{1}{Req} = \frac{1}{R_1} + \frac{1}{R_2} \qquad (1.8)$$

The equivalent resistance of two parallel resistors is equal to the product of their resistances divided by their sum.

$$\frac{1}{R_{parallel}} = \sum_{i=1}^{i=N} \frac{1}{R_i} \qquad (1.9)$$

Table 1-2 : The main characteristics of series circuit and parallel circuit

The main characteristics of series circuit are	The main characteristics of a parallel circuit are :
1. All components have the same (equal) current	1- Current through each component add to equal total current
2. voltage drops are additive.	2. All components have the same (equal) voltage
3- resistances are additive.	3. conductances are additive
4- powers are additive	4- powers are additive

1.5.2 Active elements

There are two types of sources (Voltage source and current source). Sources can be either independent or dependent upon some other quantities.

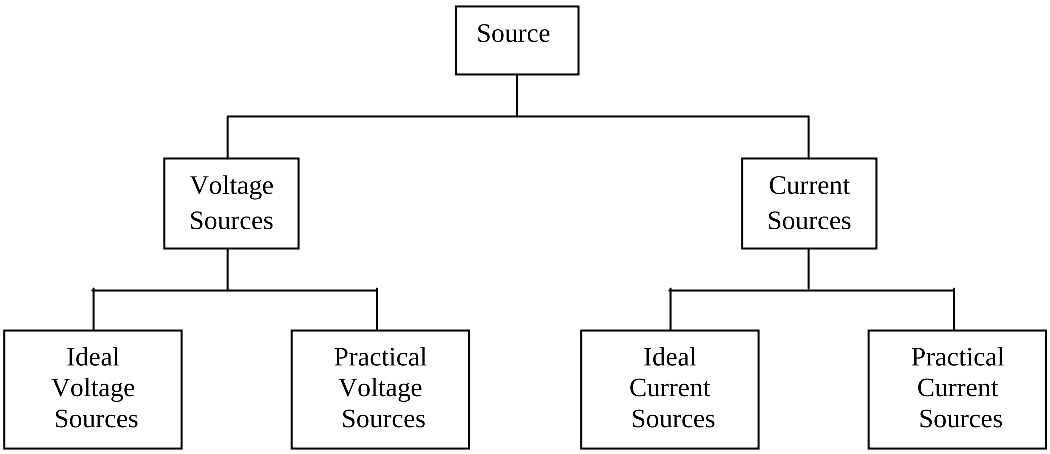
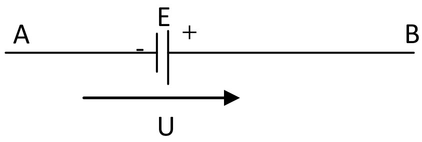


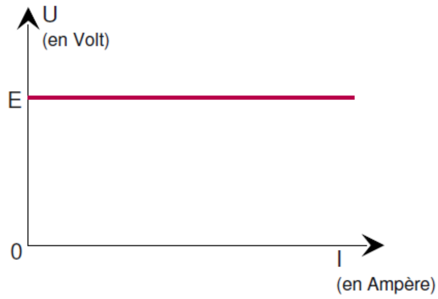
Figure 1-8 : Sources Types

1.5.2.1 The Ideal Voltage Source

An ideal voltage source, shown in figure 1-9(a), has a terminal voltage which is independent of the variations in load. In other words, for an ideal voltage source, the supply current alters with changes in load but the terminal voltage, *U* always remains constant. This characteristic is depicted in figure 1-9(b).



(a) An ideal voltage source.

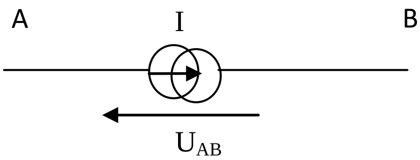


(b) characteristics of an ideal voltage source.

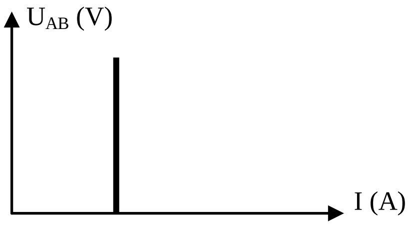
Figure 1-9 : Schematic and characteristics of an ideal voltage source

1.5.2.2 Ideal Current Source .

An ideal current source is defined as a two-terminal circuit element that supplies a constant current regardless of the voltage across it.



a) An ideal Current source.



(b) characteristics of an ideal Current source.

Figure 1-10 : Schematic and characteristics of an ideal current source

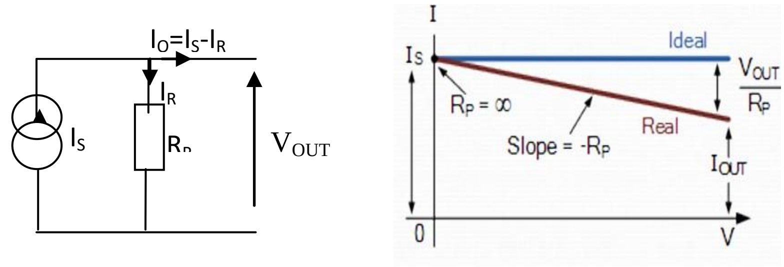
1.5.2.3 Practical Voltage Source and Practical Current Source

- ✓ **Practical Voltage Source**

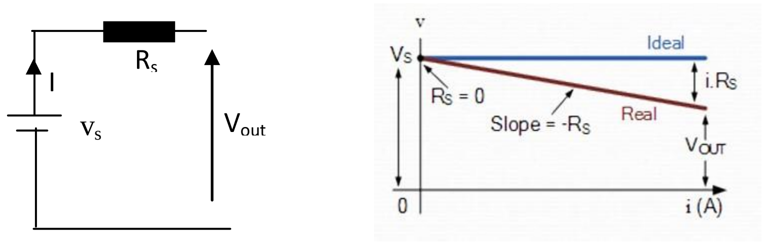
A **practical voltage source** is a real-world source that provides voltage to a circuit but also has an **internal resistance** in series with an ideal voltage source. This internal resistance causes the output voltage to **decrease slightly** when current flows (Figure 1-11.b).

- ✓ **Practical Current Source:**

A **practical current source** is a real-world source that supplies current to a circuit but has a **finite internal resistance** connected **in parallel** with an ideal current source. Because of this internal resistance, the current delivered to the load **varies slightly** with changes in load resistance (Figure 1-11.a).



(a) Practical Current Source



(b) Practical Voltage Source

Figure 1-11 : Practical Voltage Source and Practical Current Source

1.6 Circuit Theorems

1.6.1 Kirchoff's Laws

Arguably the most common and useful set of laws for solving electric circuits are the Kirchoff's voltage and current laws. Several other useful relationships can be derived based on these laws.

1.6.1.1 Kirchoff's Current Law (KCL)

The algebraic sum of all the currents entering or leaving a node in an electric circuit is equal to zero.Mathematically, KCL can be expressed as

$$\sum_{n=1}^{N} i_n = 0 \qquad (1.10)$$

where

N : is the number of branches connected to the node.

i_n: is the current in the nth branch (positive for currents entering and negative for those leaving the node).

At the node shown in Figure 1-12, applying Kirchhoff's Current Law (KCL) yields:

$$I_1 + I_2 = I_3 + I_4 + I_5 + I_6 \qquad (1.11)$$

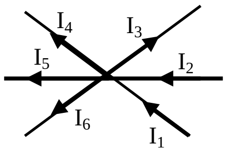


Figure 1-12 : Kirchoff's Current Law (KCL)

1.6.1.2 Kirchoff's Voltage Law (KVL)

The sum of all the voltages around a closed loop is equal to zero."

Mathematically, KVL can be expressed as:

$$\sum_{m=1}^{m} V_m = 0 \tag{1.12}$$

Where

M : is the number of voltages (or branches) in the loop,

Vm is the voltage across the m-th element.

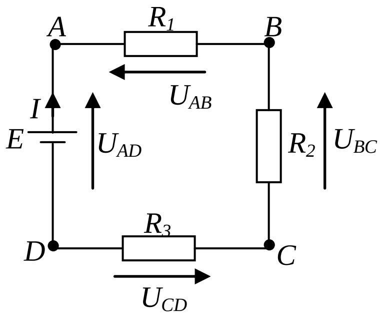


Figure 1-13 : Kirchoff's Voltage Law (KVL)

At the Loop shown in Figure 1-13, applying Kirchhoff's Voltage Law (KVL) yields:

$$V_{AD} - V_{AB} - V_{BC} - V_{CD} = 0 \tag{1.13}$$

1.6.2 Voltage Divider Rule (VDR)

The Voltage Divider Rule (VDR) states that the voltage across an element in a series circuit is equal to the resistance of the element divided by the total resistance of the series circuit and multiplied by the total impressed voltage in figure 1-14:

$$U_1 = \frac{R_1}{R_1 + R_2} E \tag{1.14}$$

$$U_2 = \frac{R_2}{R_1 + R_2} E \tag{1.15}$$

Where:

- U_1, U_2 voltage across the element or series combination,
- E: total applied voltage,
- R_1, R_2: resistance of the element or combination.

.

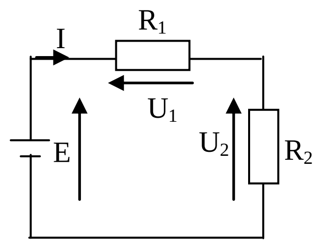


Figure 1-14 : : Voltage Divider Rule (VDR)

1.6.3 Current Divider Rule (CDR)

The **Current Divider Rule (CDR)** states that the current through one of two parallel branches is equal to the resistance of the other branch divided by the sum of the resistances of the two parallel branches and multiplied by the total current entering the two parallel branches. That is, figure 1-15:

$$I_1 = \frac{R_2}{R_2 + R_1} I_T \quad (1.16)$$

$$I_2 = \frac{R_1}{R_2 + R_1} I_T \quad (1.17)$$

Where:

1. I_T: total current entering the node,
2. I_1, I_2: currents through each branch,
3. R_1, R_2: resistances of the two parallel branches

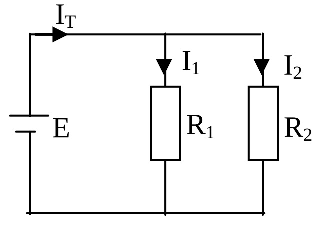


Figure 1-15 : Current Divider Rule (CDR)

1.6.4 Superposition Theorem

The **Superposition Theorem** states that in any linear circuit containing multiple independent sources (voltage or current), the current or voltage across any element can be determined by adding the individual effects of each source acting alone, with all other sources turned off during each calculation.

1.6.4.1 Steps to Apply Superposition Principle

1. Keep only one source active at a time and turn off the others:
   - Replace voltage sources with short circuits (wires).
   - Replace current sources with open circuits
2. Determine the current or voltage produced by the active source.
3. Algebraically add all the individual contributions (considering signs and directions) to obtain the total current or voltage

Example

With the help of superposition theorem, obtain the value of current i the circuit of the resistor R_2 figure 1-16.

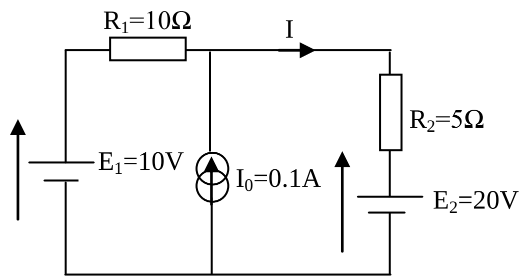


Figure 1-16 : Superposition Theorems

Solution.

As usual, we will break down the problem into three parts involving one source each

First Step: As shown in Figure. 1-17 (b), current source I_0 has been replaced by an open-circuit. the voltage source E_2 has been replaced by a short circuit.

Second Step:

As shown in Figure. 1-17 (b), the voltage source E_1 has been replaced by a short circuit. the voltage source E_2 has been replaced by a short circuit.

Third Step: As shown in figure. 1-17 (c), current source I_0 has been replaced by an open-circuit. the voltage source E_1 has been replaced by a short circuit.

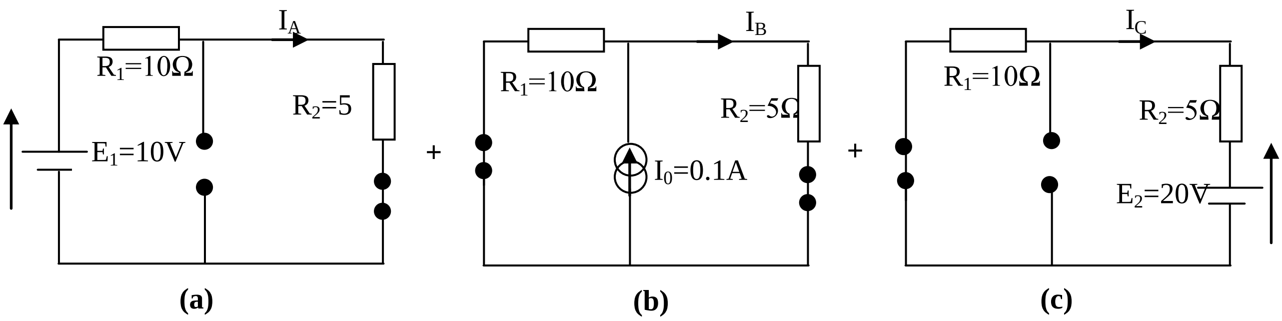


Figure 1-17 : Superposition Theorems

Figure 1-17.*a* Using KVL, we get

$$E_1 = (R_1 + R_2)I_A \Rightarrow I_A = \frac{E_1}{R_1 + R_2} = \frac{10}{10+5} = 0.66A \qquad (1.18)$$

Figure 1-17..*b* Using Current Divider principle, we get

$$I_B = \frac{R_1}{R_1 + R_2} I_0 = \frac{10}{10+5} \times 0.1 = 0.06A \qquad (1.19)$$

Figure 1-17.*c* Using KVL, we get

$$E_2 = -(R_1 + R_2)I_C \Rightarrow I_C = -\frac{E_2}{R_1 + R_2} = \frac{20}{10+5} = -1.33A \qquad (1.20)$$

Fourthly step Using Superposition principle, we get

$$I = I_A + I_B + I_C \Rightarrow I = 0.66 + 0.06 - 1.33 = -0.61A \qquad (1.21)$$

1.6.5 Noron's Theorem

Norton's theorem states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a current source I_N in parallel with a resistor R_N (Figure 1-18).

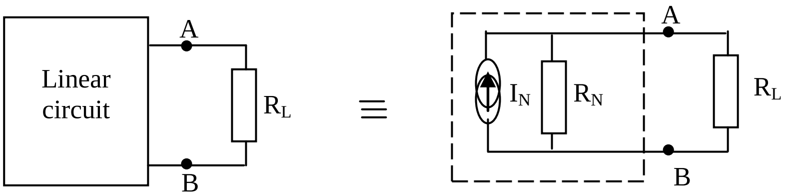


Figure 1-18 : Norton equivalent circuit

Where

- ✓ I_N is the short-circuit current through the terminals
- ✓ R_N is the equivalent resistance at the terminals when the independent sources are turned off.

1.6.5.1 How to Nortonize a given circuit ?

Step 1: Remove that portion of the network across which the norton equivalent circuit is found.

Step 2: make the terminals of the remaning two-terminal network

Step 3: Calculate R_N by first setting all sources to zero (voltage sources are replaced by short circuits, and current sources by open circuits) and then finding the resultant resistance between the two marked terminals**.**

Step 4: Calculate I_N by first returning all sources to their original position and finding the short-circuit current between the marked terminals**.**

Step 5: Draw the Norton equivalent circuit with the portion of the circuit previously removed replaced between the terminals of the equivalent circuit.

1.6.6 Thevenin's theorem

Thevenin's theorem states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a voltage source V_{Th} in series with a resistor R_{Th} (Figure 1-19).

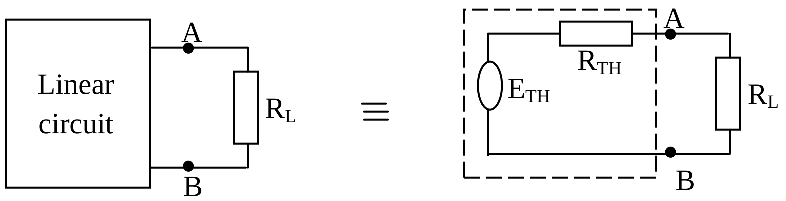


Figure 1-19 : Thevenin equivalent circuit

Where

V_{Th} is the open-circuit voltage at the terminals and

R_{Th} is the equivalent resistance at the terminals when the independent sources are turned off.

1.6.6.1 How to Thevenize a given circuit?

Step 1: Remove that portion of the network across which the Thevenine equivalent circuit is found

Step 2: make the terminals of the remaning two-terminal network

Step 3: Calculate R_{TH} by first setting all sources to zero (voltage sources are replaced by short circuits, and current sources by open circuits) and then finding the resultant resistance between the two marked terminals.

Step 4: Calculate E_{TH} by first returning all sources to their original position and finding the short-circuit current between the marked terminals.

Step 5: Draw the Thevenin equivalent circuit with the portion of the circuit previously removed replaced between the terminals of the equivalent circuit.

1.6.7 Source Transformation

A source transformation is the process of replacing a voltage source E_{TH} in series with a resistor R_{TH} by a current source I_N is in parallel with a resistor R_N, or vice versa (Figure1-20).

$$R_N = R_{TH}; \qquad R_N I_N = V_{TH} \tag{1.22}$$

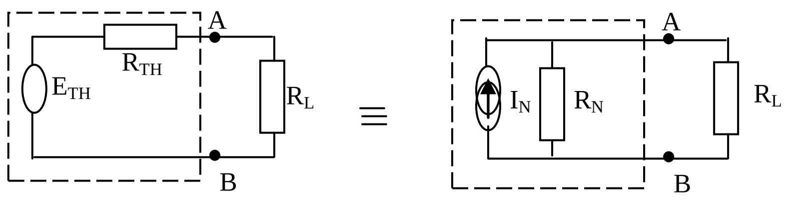


Figure 1-20 : Source Transformation

1.6.8 Delta/Star Transformation and Star/Delta Transformation

It allows for the conversion between a network of three resistors connected in a star configuration and a network of three resistors connected in a delta configuration, and vice versa

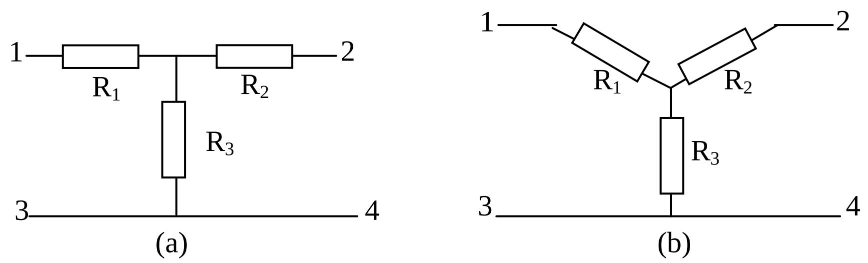


Figure 1-21 : Two forms of the same network: (a) Y, (b) T

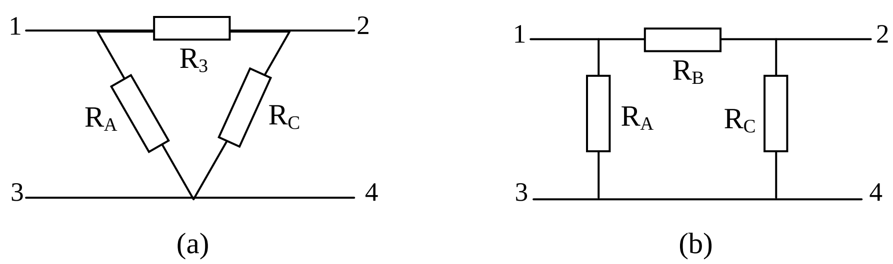


Figure 1-22 : Two forms of the same network: (a), (b)

1.6.8.1 Star/Delta Transformation

This transformation can be easily done by the following equations (Figure 1-23):

$$\Delta Y : R_1 = \frac{R_B R_C}{R_A + R_B + R_C} \tag{1.23}$$

$$\Delta Y : R_2 = \frac{R_A R_C}{R_A + R_B + R_C} \tag{1.24}$$

$$\Delta Y : R_3 = \frac{R_A R_B}{R_A + R_B + R_C} \tag{1.25}$$

.

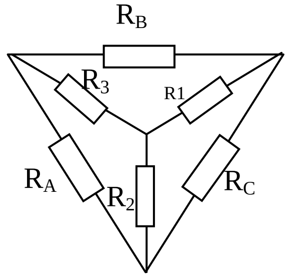


Figure 1-23 : Conversion between Y and Δ networks.
See text for conversion formulas

- **How to Remember?**

Each resistor in the Y network is the product of the resistors in the two adjacent Δ branches, divided by the sum of the three Δ resistors

1.6.8.2 Delta/Star Transformation

This transformation can be easily done by the following equations (Figure 1-22):

$$Y\Delta : R_A = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_1} \tag{1.26}$$

$$Y\Delta : R_B = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_2} \tag{1.27}$$

$$Y\Delta : R_C = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{R_3} \tag{1.28}$$

- **How to Remember?**

Each resistor in the Δ network is the sum of all possible products of Y resistors taken two at a time, divided by the opposite Y resistor.

1.6.9 Millman's theorem

Millman's theorem is a specific form of Kirchhoff's current law expressed in terms of voltage. In an electrical network with parallel branches, where each branch contains a perfect voltage source in series with a linear element, the voltage across the branches is equal to the sum of the electromotive forces, each multiplied by the conductance. of the corresponding branch, divided by the sum of the conductance (Figure 1-24).

$$V_{AB} = \frac{\sum_{i=1}^{n} \frac{E_i}{R_i}}{\sum_{i=1}^{n} \frac{1}{R_i}} \qquad V_{AB} = \frac{\sum_{i=1}^{n} E_i G_i}{\sum_{i=1}^{n} G_i} \tag{1.29}$$

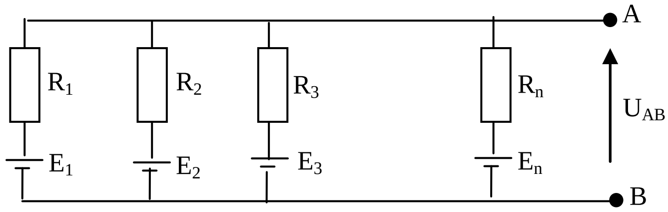


Figure 1-24 : Eample of Millman's theorem to find V_{AB}

It can also be generalized to include current sources (Figure 1-25). If there are, still in parallel, currents (such as those from current sources) known to be injected into the same point M, then it can be written as :

$$V_{AB} = \frac{\sum_{i=1}^{n} \frac{E_i}{R_i} + \sum_{J=1}^{n} I_J}{\sum_{i=1}^{n} \frac{1}{R_i}} \qquad V_{AB} = \frac{\sum_{i=1}^{n} E_i G_i + \sum_{J=1}^{n} I_J}{\sum_{i=1}^{n} G_i} \tag{1.30}$$

It is noted that the presence of current sources does not change the denominator.

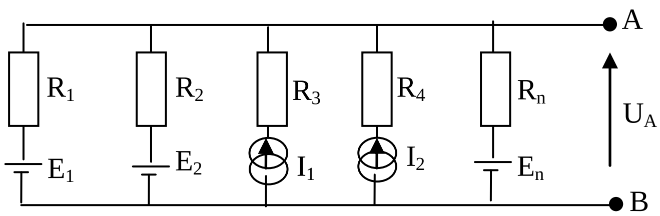


Figure 1-25 : Application du Théorème de Millman

1.6.10 Maximum Power Transfer Theorem

The maximum power transfer theorem states the following:
A load will receive maximum power from a linear bilateral DC network when its total resistive value is exactly equal to the Thévenin resistance of the network as “seen” by the load (Figure 1-26).

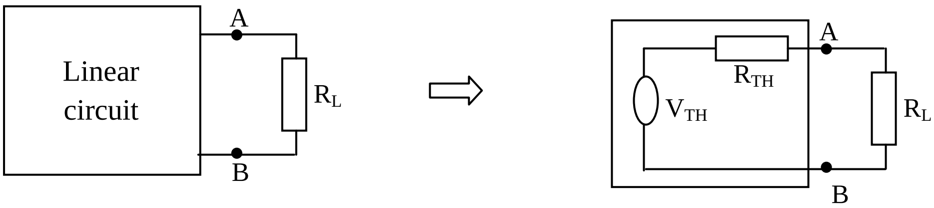


Figure 1-26 : The circuit used for maximum power transfer

According to this theorem, R_L will abstract maximum power from the network when $R_{TH} = R_L$

Circuit current

$$I = \frac{E_{TH}}{R_{TH} + R_L} \qquad (1.31)$$

Power consumed by the load is

$$P_L = V.I = R_L I^2 = R_L \left(\frac{E_{TH}}{R_{TH} + R_L} \right)^2 \qquad (1.32)$$

For P_L to be maximum $\frac{dP}{dR_L} = 0$

$$\frac{dP}{dR_L} = \frac{1}{\left[(R_{TH} + R_L)^2 \right]^2} \left((R_{TH} + R_L)^2 \frac{d}{dR_L} \left(E_{TH}^2 R_L \right) - E_{TH}^2 R_L \frac{d}{dR_L} (R_{TH} + R_L)^2 \right) \qquad (1.33)$$

$$\frac{dP}{dR_L} = \frac{1}{(R_{TH} + R_L)^4} \left((R_{TH} + R_L)^2 E_{TH}^2 - E_{TH}^2 R_L \times 2(R_{TH} + R_L) \right) \qquad (1.34)$$

$$\frac{dP}{dR_L} = \frac{E_{TH}^2 (R_{TH} + R_L)}{(R_{TH} + R_L)^4} (R_{TH} + R_L - 2R_L) \qquad (1.35)$$

$$\frac{dP}{dR_L} = \frac{E_{TH}^2}{(R_{TH} + R_L)^3} (R_{TH} - R_L) \qquad (1.36)$$

$$\frac{dP}{dR_C} = 0 \Leftrightarrow R_{CH} = R_{TH} \tag{1.37}$$

It is worth noting that under these conditions, the voltage across the load is hold the open-circuit voltage at the terminals A and B.

$$P_{Max} = \frac{(E_{TH})^2 R_{TH}}{(R_{TH} + R_{TH})^2} = \frac{(E_{TH})^2}{4R_{TH}} \tag{1.38}$$

The following figure shows the waveform of the power consumed by the load as a function of its resistance. Maximum power is obtained when the load resistance is equal to the Thévenin resistance (Figure 1-27).

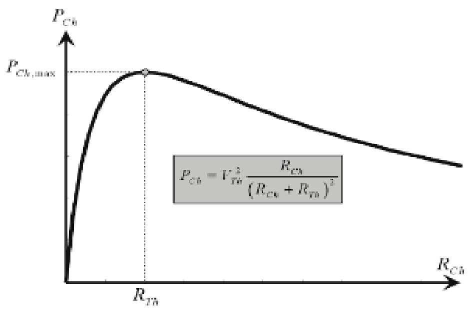
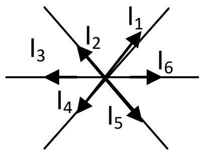
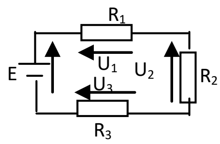
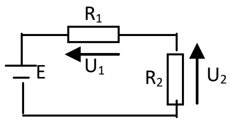
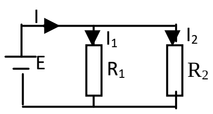
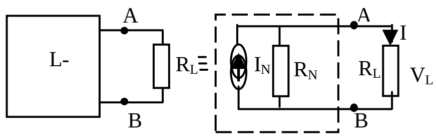
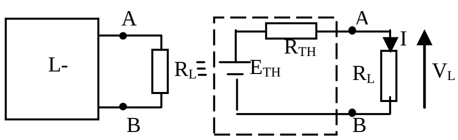
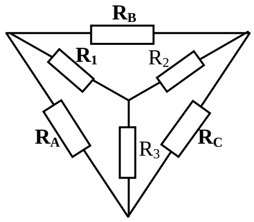
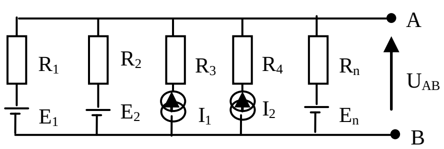
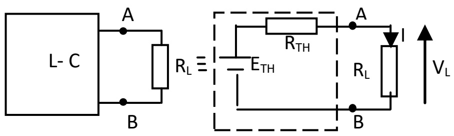


Figure 1-27 : Load power curve as a function of its resistance

Table 1-3 : Sammry DC network theorems

KCL		$\sum_{K=1}^{n} i_{kk} = 0$
KVL		$\sum_{K=1}^{n} i_{kk} = 0$
VDR		$U_1 = \frac{R_1}{R_1 + R_2} E$
CDR		$I_1 = \frac{R_2}{R_1 + R_2} I$
Norton theorem		$I = \frac{R_N}{R_N + R_L} I_N$
		$V_L = R_L I$
Thevenin theorem		$I = \frac{E_{TH}}{R_{TH} + R_L}$
		$V_L = R_L I$
Δ ⟷ Y		$R\Delta = \frac{\sum \text{all cross products in Y}}{\text{opposite R in Y}}$
		$RY = \frac{\text{product of two adjacent R in}\Delta}{\sum \text{all R in } \Delta}$
Millman theorem		$V_{AB} = \frac{\sum_{i=1}^{n} E_i G_i + \sum_{J=1}^{n} I_J}{\sum_{i=1}^{n} G_i}$
MPTT		$R_L = R_{TH}$
		$P_{Max} = (E_{TH})^2 / 4R_{TH}$

1.7 Glossary

Farncais	English	العربية
Résistance	Resistance	مقاومة
Puissance	Power	الإستطاعة
Energie	Energy	الطاقة
Courant	Current	التيار
Tension	Electric potential	التوتر
Réseau	Network	الشبكة
Nœud	Node	العقدة
Branche	Branch	الفرع
Maille	Mesh	العروة
Current Divider Rule	Diviseur de Courant	قاعدة مقسم التيار
Voltae Divider Rule	**Diviseur de Tension**	قاعدة مقسم الجهد

DC NETWORK THEOREMS

Exercises

Exercise 01.1 : Calculate the equivalent resistance

For the circuit shown in figure 1-28, calculate :

a- the equivalent resistance between the following point A and B

b- the equivalent resistance between the following point C and D

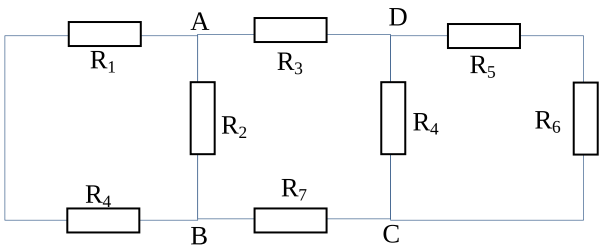


Figure 1-28 : Circuit for Exercise 01.1 .

Exercise 01.2: Kirchhoff's Laws

For the circuit shown in Figure 1-29, use Kirchhoff 's Laws to calculate (a) the current flowing in each branch of the circuit.

$E_1 = 12V, E_2 = 6V, R_1 = 8\Omega, R_2 = 12\Omega \, and \, R_3 = 4\Omega$

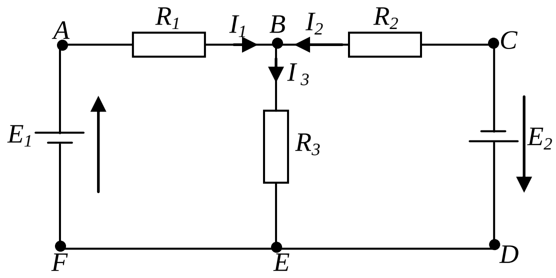


Figure 1-29 : Circuit for Exercise 01.2

Exercise 01.3: Current Divider Rule / Potential Divider Rule

Considering the circuit of figure 1-30 calculated,

a- The current drawn from the source

b- The currents I_1 and I_2 using the Current divider

c- The Potentials U_4 and U_5 using the voltage divider

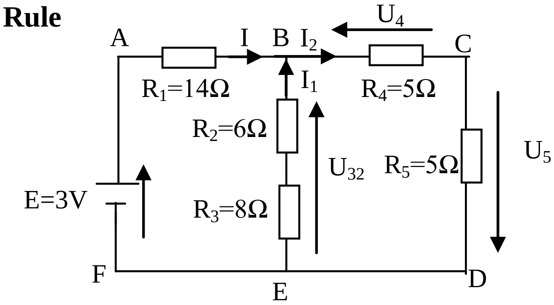


Figure 1-30 : Circuit for Exercise 01. 3

Exercise 01.4: Thevenin's Theorem and Norton's theorem

Considering the circuit of figure 1-31:

Determine the current flowing through resistor R_L

a- by using Norton's theorem.

b- by using thevenin's theorem

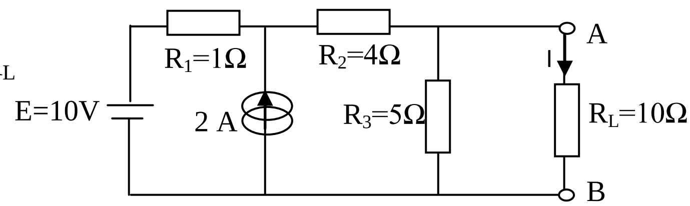


Figure 1-31 : Circuit for Exercise 01.4

Exercise 01.5: Star/delta transformations

Calculate the current flowing through the of Figure 1-32 by using any method.

$E = 12V, R_1 = R_2 = R_3 = 6\Omega \;\; and \;\; R_A = R_B = R_C = 9\Omega$

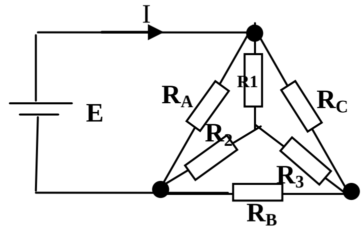


Figure 1-32 : Circuit for Exercise 01.5

Exercise 01.6 : Millman Theorem

Use Millman's theorem, to find the common voltage across terminals M and N and the load current in the circuit of Figure. 1-33.

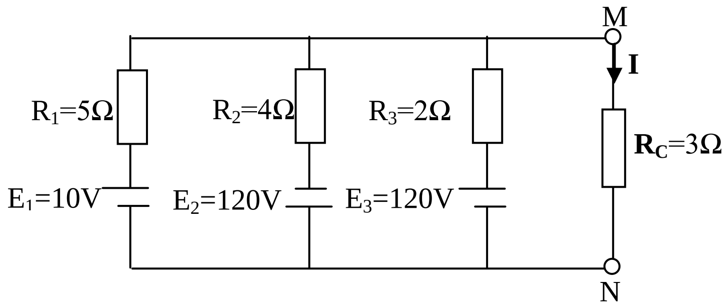


Figure 1-33 : Circuit for Exercise 01.6

Exercise 01.7: Maximum Power Transfer Theorem

Consider the network in Figure 1-34

a- Determine the value of the resistance R_L allowing maximum power transfer.

b- Then calculate the power supplied to this resistance

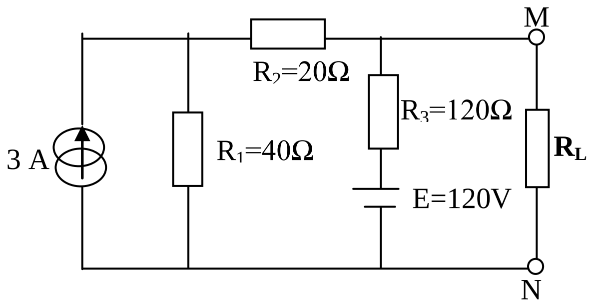


Figure 1-34 : Circuit for Exercise 01.7

DC NETWORK THEOREMS

Solutions

Exercise 01.1 : Calculate the equivalent resistance

a- The equivalent resistance between the following point A and B

To determine the total resistance of the circuit, we need to look at the combination of the resistors in series and in paralle.

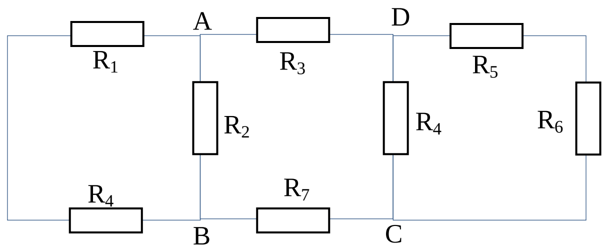


Figure 1.27

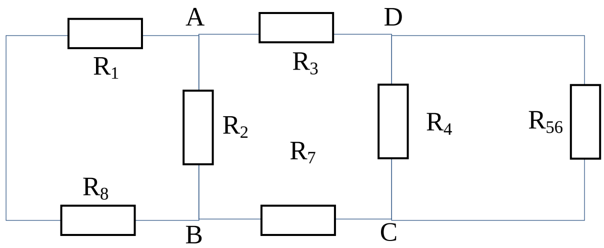


Figure 1-27.a

In the circuit $\mathbf{R_5}$ and $\mathbf{R_6}$ are in **series (Figure 1-27.a)** :

$$R_{56} = R_5 + R_6 = 5 + 5 = 10\Omega$$

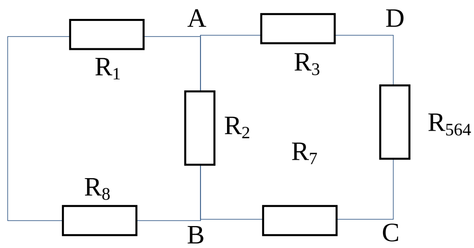


Figure 1-27.b

$\mathbf{R_{56}}$ and $\mathbf{R_4}$ **are in** parallel (**Figure 1.27.b)**

$$R_{564} = \frac{R_{56} \times R_4}{R_{56} + R_4} = \frac{10 \times 5}{10 + 5} = 3.33\Omega$$

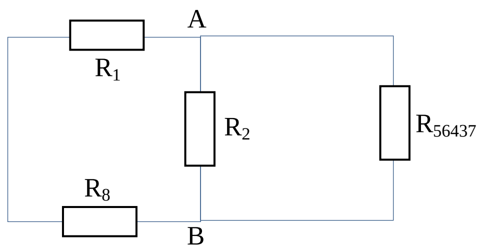


Figure 1-27.c

R_{564} R_3 and R_7 are in series (**Figure 1-27.c)**

$$R_{56437} = R_{564} + R_3 + R_7 = 3.33 + 5 + 5 = 13.33\Omega$$

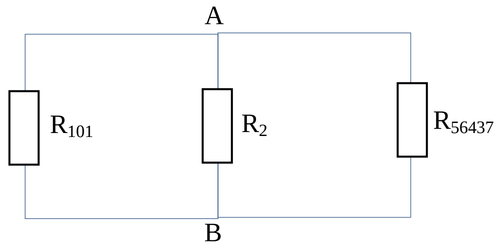


Figure 1-7.d

R_1 and R_{10} are in series (**Figure 1-27.d)**

$$R_{101} = R_1 + R_{10} = 5 + 5 = 10\Omega$$

The equivalent resistance between the following point A and B (**Figure 1-27.e)**

$$R_{AB} = \frac{R_{56437} \times R_2 \times R_{101}}{R_{56437} \times R_2 + R_{101} \times R_2 + R_{101} \times R_{56437}} = \frac{13.33 \times 5 \times 10}{13.33 \times 5 + 10 \times 5 + 10 \times 13.33} = 2.66\Omega$$

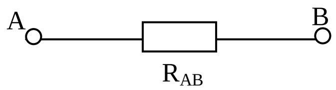


Figure 1-27.e

b- The equivalent resistance between the following point B and C

We can save a lot of time in this second part by using the principle of symmetry. Indeed, if the circuit were rotated around its transverse axis in such a way that points A and B become points C and D, as shown in the figure below, the circuit would remain unchanged. Thus, the resistance of the circuit as seen from terminals C and D is the same as that seen from terminals A and B, which we analyzed in the previous question. Therefore, the resistance is $R_{CD} = 2.66\Omega$.

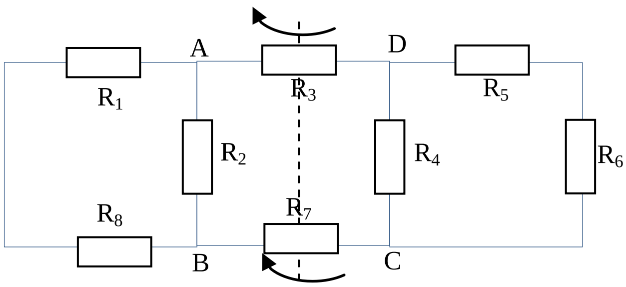
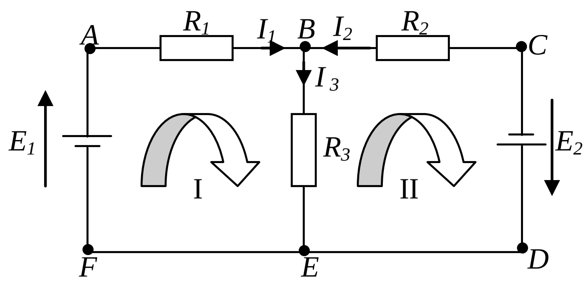


Figure 1-27.f

Exercise 01.3: Kirchhoff ' s Laws



Applying KCL to node B, we get:

$I_1 + I_2 - I_3 = 0 \qquad I_1 + I_2 = I_3$

Applying KVL to node B, we get:

$$E_1 - R_1 I_1 - R_3 I_3 = 0$$

Applying KCL to node B, we get:

$$I_1 + I_2 - I_3 = 0$$

$$\begin{cases} R_1 I_1 + R_3 I_3 = E_1 \\ -R_3 I_3 - R_2 I_2 = E_2 \end{cases}$$

$$I_1 = I_3 - I_2$$

$$\begin{cases} R_1(I_3 - I_2) + R_3 I_3 = E_1 \\ R_2 I_2 + R_3 I_3 = -E_2 \end{cases}$$

$$\begin{cases} R_1 I_3 - R_1 I_2 + R_3 I_3 = E_1 \\ R_2 I_2 + R_3 I_3 = -E_2 \end{cases}$$

$$\begin{cases} -R_1 I_2 + (R_1 + R_3) I_3 = E_1 \\ R_2 I_2 + R_3 I_3 = -E_2 \end{cases}$$

$$\begin{cases} -8 I_2 + (8 + 4) I_3 = 12 \\ 12 I_2 + 4 I_3 = -6 \end{cases}$$

$$\begin{cases} -8 I_2 + 12 I_3 = 12 \\ 12 I_2 + 4 I_3 = -6 \end{cases}$$

$$\begin{bmatrix} -R_1 & R_1 + R_3 \\ R_2 & R_3 \end{bmatrix} \begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} E_1 \\ -E_2 \end{bmatrix} \qquad \begin{bmatrix} -8 & 12 \\ 12 & 4 \end{bmatrix} \begin{bmatrix} I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 12 \\ -6 \end{bmatrix}$$

We obtain the determinants

$$\Delta R = \begin{bmatrix} -R_1 & R_1 + R_3 \\ R_2 & R_3 \end{bmatrix} = (-R_1)(R_3) - (R_2)(R_1 + R_3)$$

$$\Delta R = \begin{bmatrix} -8 & 12 \\ 12 & 4 \end{bmatrix} = (-8)(4) - (12)(12) = -32 - 144 = -176$$

Thus

$$I_2 = \frac{\begin{bmatrix} E_1 & R_1 + R_3 \\ -E_2 & R_3 \end{bmatrix}}{\Delta R} \qquad I_2 = \frac{\begin{bmatrix} 12 & 12 \\ -6 & 4 \end{bmatrix}}{-176} = \frac{12 \times 4 - (-6 \times 12)}{-176} = \frac{48 + 72}{-176} = -0{,}68 A$$

$$I_3 = \frac{\begin{bmatrix} R_1 & E_1 \\ R_2 & -E_2 \end{bmatrix}}{\Delta R} \qquad I_3 == \frac{\begin{bmatrix} 8 & 12 \\ 12 & -6 \end{bmatrix}}{\Delta R} = \frac{-6 \times 8 - (12 \times 12)}{-176} = \frac{48 - 144}{-176} = 0{,}54 A$$

Finally

$$I_1 = I_3 - I_2 = 0.54 - (-0.68) = 1.22\,A$$

Exercise 01.3: Current Divider Rule/ Potential Divider Rule

The equivalent resistance Between the following point A and F

To determine the total resistance of the circuit, we need to look at the combination of the resistors in series and in paralle.

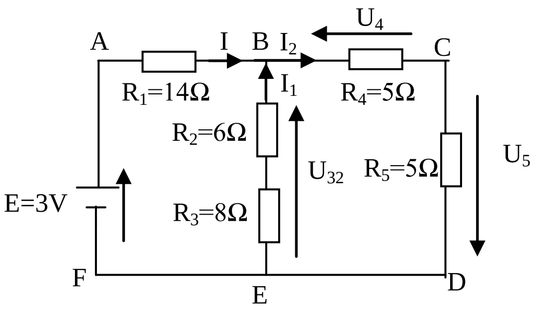


Figure 1-29

Resistors $\mathbf{R_4}$ and $\mathbf{R_5}$ are acting in **series**, so we add their resistances up to find (**Figure 1-29.a) :**

$$R_{é1} = R_4 + R_5 = 5 + 5 = 10\Omega$$

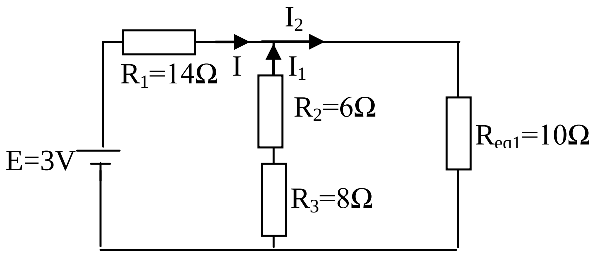


Figure 1-29.a

Resistors $\mathbf{R_2}$ and $\mathbf{R_3}$ are acting in **series**, so we add their resistances up to find(**Figure 1-29.b)**:

$$R_{é2} = R_3 + R_2 = 6 + 8 = 14\Omega$$

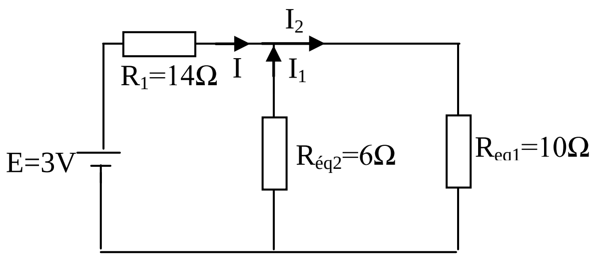


Figure 1-29.b

The equivalent resistor $\mathbf{Req_1}$ is acting in **parallel** with the equivalent resistor $\mathbf{R_{eq2}}$ and to find the equivalent resistor Req_3 (**Figure 1-29.c)**we use:

$$R_{é3} = \frac{R_1 \times R_{é2}}{R_1 + R_{é22}} = \frac{10 \times 14}{10 + 14} = 5.83\Omega$$

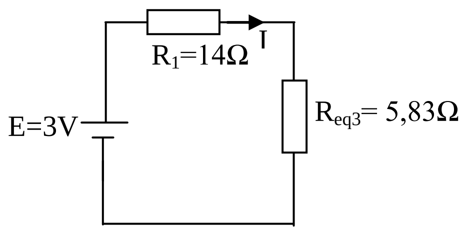


Figure 1-29.c

The equivalent resistor $\mathbf{Req_3}$ is acting in sersis with the equivalent resistor $\mathbf{R_1}$ and to find the total resistance $\mathbf{R_{AF}}$ **(Figure 1-29.b)**

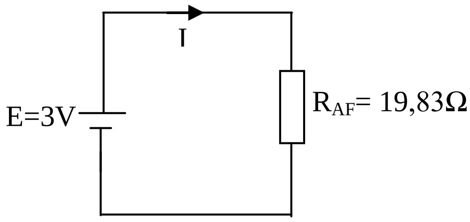


Figure 1-29.c

$$R_{AF} = R_1 + R_{é3} = 14 + 5.83 = 19.83\Omega$$

C- The current I drawn from the source

Applying KVL to the mesh, we get (Figure 1-29.d)

$$E = R_{AF} I \Rightarrow I = \frac{E}{R_{AF}} = \frac{3}{19.83} = 0.15.A$$

C- The currents I_1 and l_2 using the Current divider

Using Current Divider principle, we get (Figure 1-29.b)

$$I_1 = -\frac{R_{éq1}}{R_{éq1} + R_{éq2}} I = -\frac{10}{10+14} 0.15. = -0.0625A$$

$$I_2 = \frac{R_{éq2}}{R_{éq1} + R_{éq2}} I = \frac{14}{10+14} 0.15. = -0.0857A$$

D- The Potentials U_2 et U_3 using the voltage divider

Using Voltage Divider principle, we get (Figure 1-29)

$$U_5 = -\frac{R_5}{R_5 + R_4} U_{23}$$

Using Voltage Divider principle, we get (Figure 1-29.c)

$$U_{23} = \frac{R_{éq3}}{R_{éq3} + R_1} E = -\frac{5.83}{5.83+14} 3. = 0.88V$$

$$U_5 = -\frac{5}{5+5} 0.88 = -0.44V$$

$$U_4 = \frac{5}{5+5} 0.88 = 0.44V$$

Exercise 01.4 : Thevenin's Theorem and Norton's theorem

A- Norton's theorem

Step 1 and **2** produce the network of Figure 1-30.a. Note that de load resistor R_L has been removed and the two ''holding'' terminals have been defined as A and B

Using Voltage Divider principle, we get (Figure 1-30.a)

$$I = \frac{R_N}{R_N + R_L} I_N$$

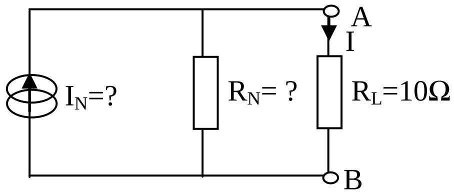


Figure 1-30.a

Step 3: remplacing the voltage source E withe a short-circuit equivalent and the resistance determined between terminals A and B

$$R_N = (R_1 + R_2) // R_3$$

$$R_N = \frac{(R_1 + R_2) \times R_3}{(R_1 + R_2) + R_3} = \frac{(1+4) \times 5}{(1+4)+5} = \frac{25}{10} = 2.5\Omega$$

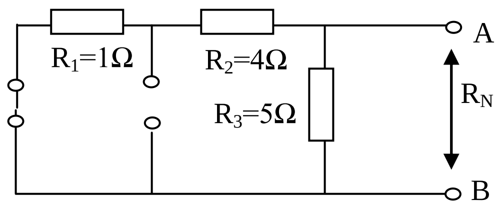


Figure 1-30.b

Step 4: To find we short-circuit terminals a and b, as shown in figure 1.30.c. We ignore the resistor R_3 because it has been short-circuited.

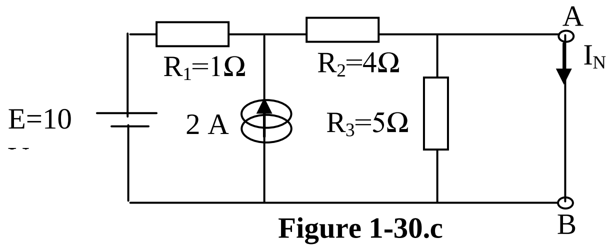


Figure 1-30.c

Applying mesh analysis, we obtain

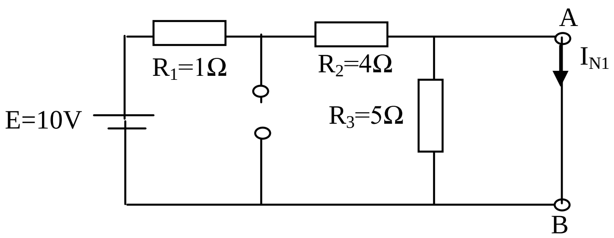


Figure 1-30.c1

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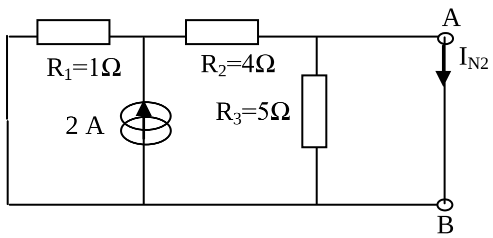

Figure 1-0.c2

Figure 1-30.c1

Applying KVL to the mesh, we get

$$E = (R_1 + R_2) I_{N1} \Rightarrow I_{N1} = \frac{E}{R_1 + R_2} = \frac{10}{1+4} = 2A$$

Figure 1-30.c2

Using Current Divider principle, we get

$$I_{N2} = \frac{R_1}{R_1 + R_2} A = \frac{1}{1+4} 2. = 0.4A$$

$$I_N = I_{N1} + I_{N2}. = 2 + 0.4 = 2.4A$$

Step 5: Is shown in figure 1-30.d

$$I = \frac{R_N}{R_N + R_2} I_N = \frac{2.5}{.2.5 + 10} 2.4 = 0.48A$$

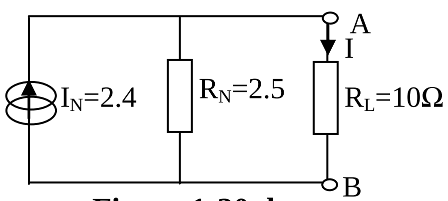

Figure 1-30.d

B-Thevenin's theorem

Step 1 and **2** produce the network of figure 30.e Note that de load resistor Rch has been removed and the two ''holding'' terminals have been defined as A and B

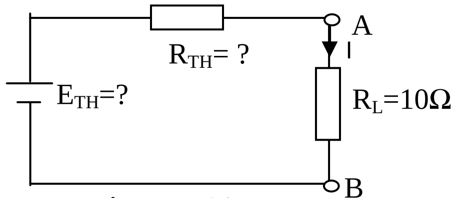

Figure 1-30.e

Applying KVL to the mesh, we get

$$E_{TH} = (R_{TH} + R_L)I \Rightarrow I = \frac{E}{R_{TH} + R_L}$$

Step 3: remplacing the voltage source E withe a short-circuit equivalent and the resistance determined between terminals A and B

$$R_{TH} = (R_1 + R_2) // R_3 = R_N = 2.5\Omega$$

Step 4: To find we short-circuit terminals a and b, as shown in figure 1.30.f. We ignore the resistor R_3 because it has been short-circuited.

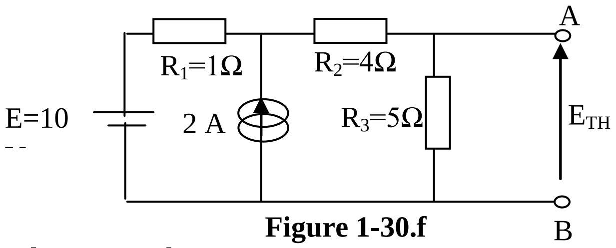

Figure 1-30.f

Applying mesh analysis, we obtain

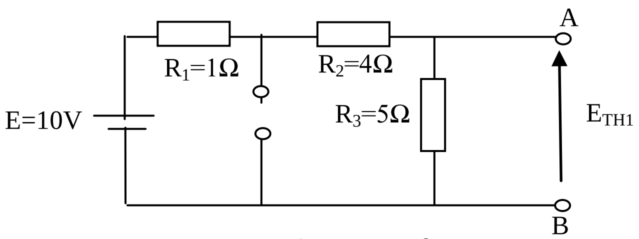

Figure 1-30.f1

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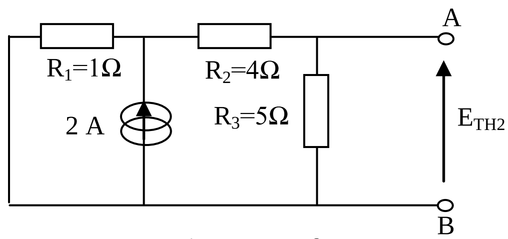

Figure 1-30.f2

Figure 1-30.f1

Using Voltge Divider principle, we get

$$E_{TH1} = \frac{R_3}{R_1 + R_2 + R_3} E = \frac{5}{1+4+5} 10. = 5V$$

.

Figure 1-30.f2

Applying KVL to the mesh, we get

$$E_{TH2} = R_3 I$$

Using Current Divider principle, we get

$$I = \frac{R_1}{R_1 + R_2 + R_3} A$$

$$I = \frac{1}{1+4+5} 2. = 0.2A$$

$$E_{TH2} = R_3 I = 5 \times 0.2 = 1V$$

$$E_{TH} = E_{TH1} + E_{TH2}. = 5 + 1 = 6V$$

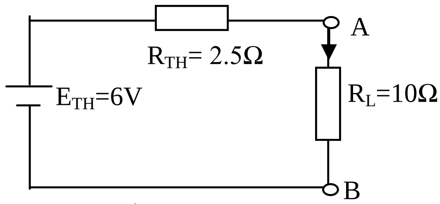

Figure 1-30.g

Step 5: Is shown in figure 1-30.g

Applying KVL to the mesh, we get

$$E_{TH} = (R_{TH} + R_L)I \Rightarrow I = \frac{E_H}{R_{TH} + R_L} = \frac{6}{10 + 2.5} = 0.48V$$

Exercise 01.5: Star/delta transformations

1. First Methode

Star/Delta Transformation Y[R1 , R2 et R3] - Δ

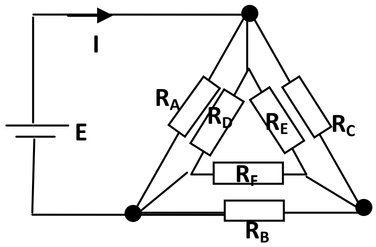

Figure 1-31.a

$$R_D = \frac{R_1R_3 + R_3R_2 + R_1R_2}{R_3}$$

$$= \frac{9*9 + 9*9 + 9*9}{9} = 27\Omega$$

$$R_D = R_E = R_F = 27\Omega$$

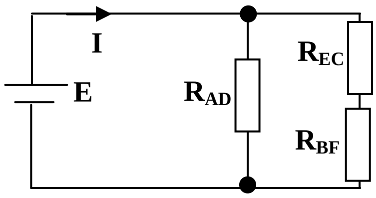

Figure 1-31.b

Figure 1.31.b:

R_E and R_C are in parallel

$$R_{EC} = \frac{R_E R_C}{R_C + R_E} = R_{AD} = R_{BF} = \frac{27*6}{27+6} = 4{,}9\Omega$$

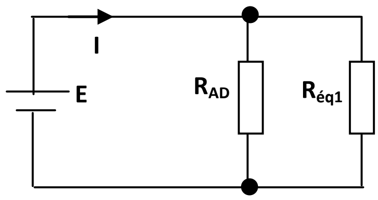

Figure 1-31.c

Figure 1.31.c

R_{BC} and R_{BF} are in serice

$$R_{éq1} = R_{EC} + R_{BF} = 4.9 + 4.9 = 9.8\Omega$$

Figure 1.31.d

The equivalent resistance between the following point A and B

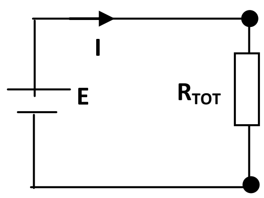

Figure 1-31.d

$$R_{TOT} = \frac{R_{AD}R_{éq}}{R_{AD} + R_{éq}} = \frac{4{,}9*9{,}8}{4{,}9+9{,}8} = 3{,}2\Omega$$

$$I = \frac{E}{R_{TOT}} = \frac{12}{3.2} = 3.75A$$

2-Second Methode

Delta/Star* Transformation $\Delta[\,R_A\,, R_B \text{ et } R_C\,]\text{-}Y$

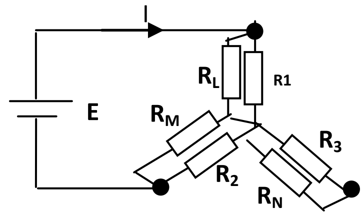

Figure 1-31.e

$$R_M = \frac{R_A R_B}{R_A + R_B + R_C} = \frac{6*6}{18} = 2\Omega$$

$$R_M = R_N = R_L = 2\Omega$$

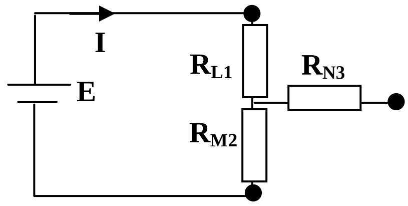

Figure 1-31.f

R_{L1} and R_{M2} are in parallel

$$R_{L1} = \frac{R_L R_1}{R_L + R_1} = \frac{9*2}{9+2} = R_{M2} = R_{N3} = 1{,}6\Omega$$

The equivalent resistance between the following point A and B

$$R_{TOT} = R_{L1} + R_{M2} = 1.6 + 1.6 = 3{,}2\Omega$$

$$I = \frac{E}{R_{TOT}} = \frac{12}{3.2} = 3.75A$$

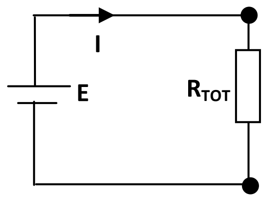

Figure 1-31.g

Exercise 01.6 : Millman Theorem's

The common voltage across terminals M and N and the load current in the circuit of Figure 1-32

The minus sign is used for E_2/R_2 because that supply has the opposite polarity of the other two. The chosen reference direction is therefore that of E_1 and E_3. The total conductance is unaffected by the direction, And

$$V_L = \frac{\dfrac{E_1}{R_1} - \dfrac{E_2}{R_2} + \dfrac{E_3}{R_3} + \dfrac{0}{R_L}}{\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_3} + \dfrac{1}{R_L}} = \frac{2-4+4+0}{0{,}20+0{,}25+0{,}25+0{,}33} = 1{,}563\ V$$

$$I_L = \frac{V_L}{R_L} = \frac{1{,}563}{3} = 0{,}521A$$

Exercise 01.7 : Maximum Power Transfer Theorem

Determine the value of $\mathbf{R_L}$ that will draw the maximum power from the rest of the circuit in figure 1-33.

We need to find the Thevenin resistance and the Thevenin voltage across the terminals a-b. To get we use the circuit in figure 1-33.a and obtain

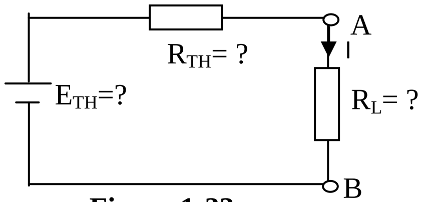

Figure 1-33.a

A- **Calculate R_{TH}**

$$R_{TH} = (R_1 + R_2) // R_3$$
$$= \frac{60 \times 120}{60 \times 120} = \frac{7200}{180} = 40\Omega$$

$$R_{TH} = R_L = 40\Omega$$

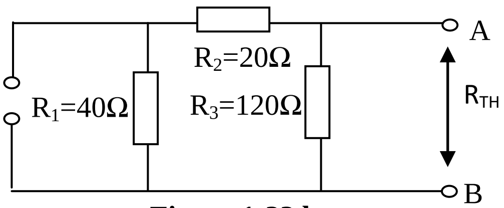

Figure 1-33.b

Calculate the maximum power

To find we short-circuit terminals a and b, as shown in figure 1-33.c. We ignore the resistor R_3 because it has been short-circuited.

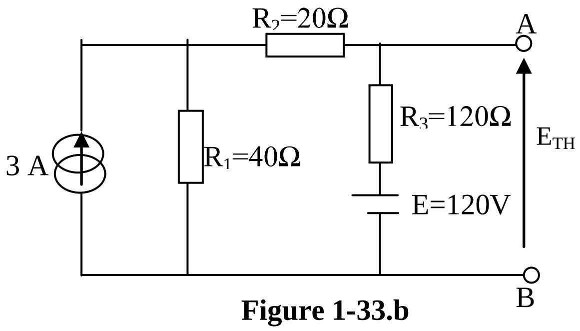

Figure 1-33.b

Using Superposition principle, we get

A=3A et E=0V **A=0A et E=120V**

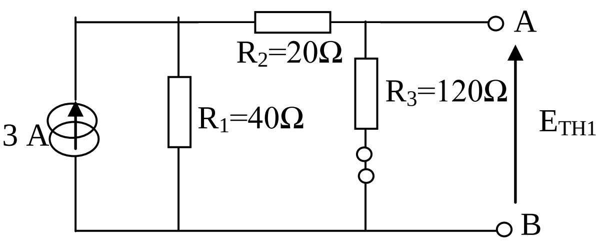

Figure 1-33.b1

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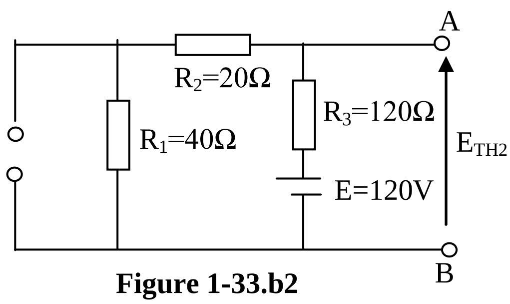


Figure 1-33.b2

Figure 1-33.b1

Applying KVL to the mesh, we get

$$E_{TH1} = R_3 I_3$$

Using Current Divider principle, we get:

$$I_3 = \frac{R_1}{R_1 + R_2 + R_3} 3 = \frac{120}{180} = 0,66A$$

$$E_{TH1} = R_3 I_3 = 120 \times 0,66 = 79,2V$$

Figure 1-33.b2

Applying KVL to the mesh, we get

$$E_{TH2} = E - R_3 I$$

$$E = (R_1 + R_2 + R_3) I$$

$$\Rightarrow I = \frac{E}{R_1 + R_2 + R_3} = \frac{120}{180} = 0,66A$$

$$E_{TH2} = 120 - 120 \times 0,66 = 40,8V$$

$$E_{TH} = E_{TH1} + E_{TH1} = 79,2 + 40,8V = 120V$$

$$P_{Max} = \frac{(E_{TH})^2}{4R_{TH}} = \frac{120^2}{4 \times 40} = 90W$$

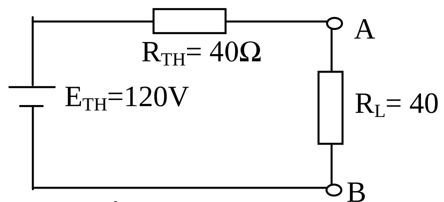


Figure 1-33.c

Chapter 02

TWO-PORT NETWORKS

2 TWO-PORT NETWORKS

Learning Objectives

By studying this chapter and completing the related exercises, you will be able to:

1. Understand the concept of a two-port network and an (N)-port network.
2. Identify and define the different parameters used in two-port network analysis.
3. Understand the relationships and interrelations between two-port network parameters.
4. Determine the conditions of reciprocity and symmetry in two-port networks.
5. Analyze the interconnection of two-port networks.
6. Study the characteristics of terminated two-port networks.
7. Understand the concept and purpose of electrical filters.
8. Identify the different types of filters and their applications.
9. Understand the concepts of bandwidth and cut-off frequency.
10. Interpret and analyze Bode plots.
11. Analyze the operation and characteristics of low-pass and high-pass filters.

2.1 What is two-port network ?

A two-port network is an electrical network with two separate ports for input and output (figure 2-1). The most general description of a linear two-port is expressed in the s-domain with variables V_I, V_O, I_I and I_O.

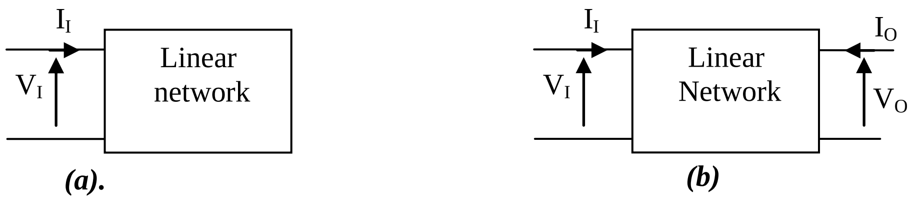


Figure 2-1 : a) One-port network, (b) two-port

2.1.1 What is N port network ?

A network having N numbers of ports; is called N port network (Figure 2-2).

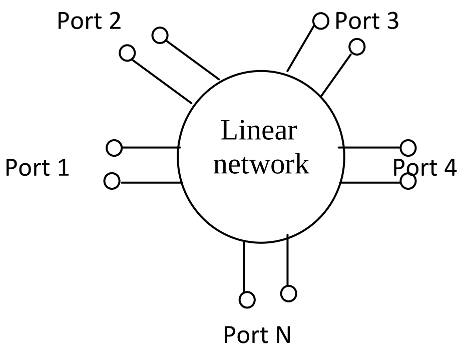


Figure 2-2 : N port network

2.2 The two ports parametres

There are various parameters needed to analyze a Two-Port network. For examples :

- Z parametres
- Y parametres
- H parametres
- G parametres
- ABCD parametres
- abcd parametres

2.2.1 Z parametres

Z Parameters Known as **impedance parameters**, Z parameters represent voltages as functions of currents in Two-Port network analysis and the units is ohm (Ω). The voltages are represented as:

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2 \qquad (2.1)$$

In matrix form as:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad (.2.2)$$

The values of the parameters can be evaluated by setting I_1=0 (input port open-circuited) or I_2=0 (output port open-circuited) Table 2-1.

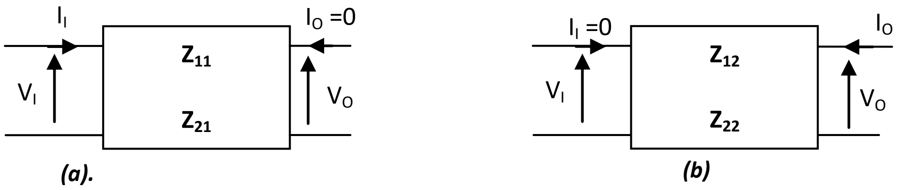


Figure 2-3 : Determination of the z parameters: (a)finding Z_{11} and Z_{21},

Table 2-1 : The values of the Z parameters

$Z_{11} = \left(\frac{V_1}{I_1}\right)_{I_2=0}$	open – circuit input impedance	$[\Omega]$.
$Z_{12} = \left(\frac{V_1}{V_2}\right)_{I_1=0}$	open – circuit transfer impedance port 1 to from port 2.	$[\Omega]$.
$Z_{21} = \left(\frac{V_2}{I_1}\right)_{I_2=0}$	open – circuit transfer impedance from port 2 to port 1.	$[\Omega]$.
$Z_{22} = \left(\frac{V_2}{i_2}\right)_{I_1=0}$	open – circuit output impedance.	$[\Omega]$.

2.2.1.1 Equivalent Circuit of Z-Parameters:

Figure 2-4 shows the impedance model of a two-port network.

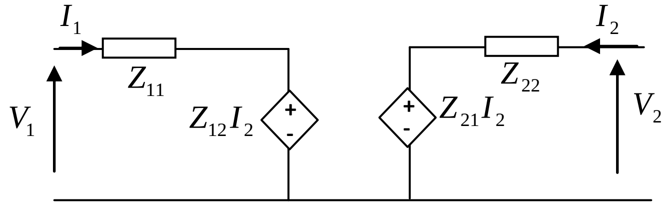


Figure 2-4 : Equivalent Circuit of Z-Parameters

2.2.2 Y Parameters

Y Parameters: Known as admittance parameters , In a Two-Port network, the input currents I_I and I_O can be expressed in terms of input and output voltages V_I and V_O respectively as [I] = [Y] [V]

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + y_{22}V_2 \qquad (2.3)$$

In matrix form as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (2.4)$$

The values of the parameters can be determined by setting (input port short-circuited) or (output port short-circuited) Table 2-2.

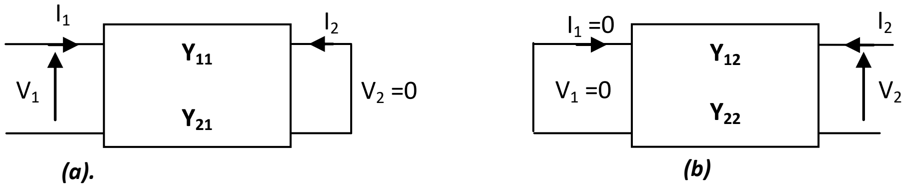


Figure 2-5 : : Determination of the Y parameters: (a)finding Y_{11} and Y_{21},

Table 2-2 : The value of Y parametres

$Y_{11} = \left(\frac{I_1}{V_1}\right)_{V_2=0}$	Short-circuit input admittance	$[\Omega^{-1}]$
$Y_{12} = \left(\frac{I_1}{V_2}\right)_{V_1=0}$	Short-circuit transfer admittance from port 2 to port 1.	$[\Omega^{-1}]$
$Y_{21} = \left(\frac{I_2}{V_1}\right)_{V_2=0}$	Short-circuit transfer admittance from port 1 to port 2.	$[\Omega^{-1}]$
$Y_{22} = \left(\frac{I_2}{V_2}\right)_{V_1=0}$	Short-circuit Ouput admittance	$[\Omega^{-1}]$

2.2.2.1 Equivalent Circuit of Y-Parameters

Figure 2-6 shows the admittance model of a two-port network.

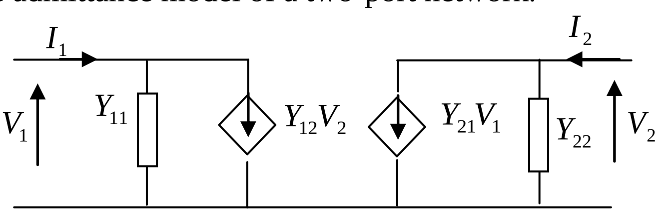


Figure 2-6 : Equivalent Circuit of Y-Parameters

2.2.3 H Parameters

The Z and Y-parameters of a two-port network do not always exist. A Two-Port network can be represented using the h-parameters. The two-port equations in terms of the hybrid parameters are

$$V_1 = H_{11}I_1 + H_{12}V_2$$
$$I_2 = H_{21}I_1 + H_{22}V_2 \qquad (2.5)$$

In matrix form as:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \qquad (2.6)$$

The values of the parameters can be determined by setting I_1=0 (input port open-circuited) or V_2=0 (output port short-circuited) Table 2-3

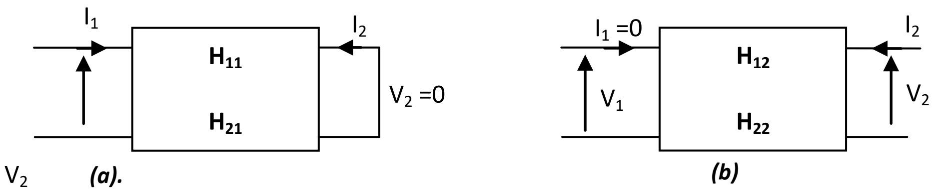


Figure 2-7 : Determination of the H parameters: (a)finding H_{11} and H_{21},

Table 2-3 : The value of H Parameters

$H_{11} = \left(\dfrac{V_I}{I_I}\right)_{V_{Os}=0}$	Short-circuit input impedance	$[\Omega]$
$H_{12} = \left(\dfrac{V_I}{V_O}\right)_{I_I=0}$	Open-circuit reverse voltage gain	dimensionless
$H_{21} = \left(\dfrac{I_O}{I_I}\right)_{V_O=0}$	Short-circuit forward current gain	dimensionless
$H_{22} = \left(\dfrac{I_O}{V_O}\right)_{I_I=0}$	Open-circuit output admittance	$[\Omega^{-1}]$

2.2.3.1 Equivalent Circuit of H –Parameters

Figure 2-8 shows the hybrid model of a two-port network.

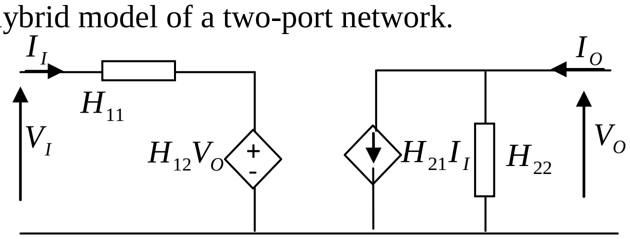


Figure 2-8 : Equivalent Circuit of H -Parameters

2.2.4 G Parameters

A set of parameters closely related to the *h* parameters are the *g* parameters or inverse hybrid parameters. These are used to describe the terminal currents and voltages as

$$I_1 = G_{11}V_1 + G_{12}I_2$$
$$V_2 = G_{21}V_1 + G_{22}I_2 \qquad (2.7)$$

In matrix form as:

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \qquad (2.8)$$

The values of the parameters can be determined by setting V_1=0 (input port short-circuited) or I_2 =0 (output port open-circuited) Table 2-4.

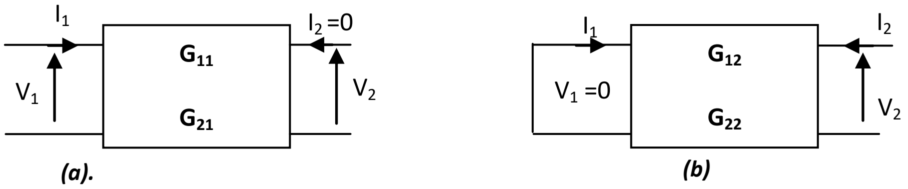


Figure 2-9 : Determination of the G parameters: (a)finding G_{11} and G_{21}, (b) finding $G_{12}$and G_{22}.

Table 2-4 : The value of G Parameters

$G_{11} = \left(\frac{I_1}{V_1}\right)_{I_2=0}$	Open-circuit input idmittance	$[\Omega^{-1}]$
$G_{12} = \left(\frac{I_1}{I_2}\right)_{V_1=0}$	Short-circuit reverse current gain	dimensionless
$G_{21} = \left(\frac{V_2}{V_1}\right)_{I_2=0}$	Open-circuit forward voltage gain	dimensionless
$G_{22} = \left(\frac{V_2}{I_2}\right)_{V_1=0}$	Short-circuit output impedance	$[\Omega]$

2.2.4.1 Equivalent Circuit of G -Parameters

Figure 2-10 shows the g-parameter model of a two-port network.

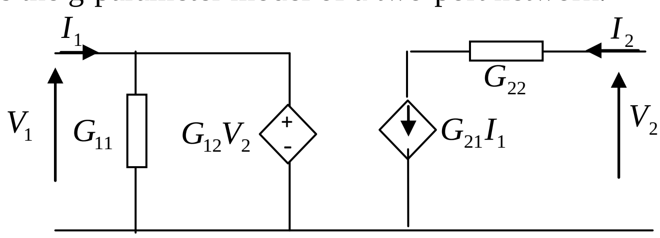


Figure 2-10 : Equivalent Circuit of G -Parameters

2.2.5 T (ABCD) Parameters

ABCD parameters are used to model transmission lines in a two-port network, linking input and output voltages and currents.

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_2 - DI_2 \qquad (2.9)$$

In matrix form as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad (2.10)$$

The values of the parameters can be determined by setting V_2 (ouput port short-circuited) or I_2 (output port open-circuited) Table 2-5.

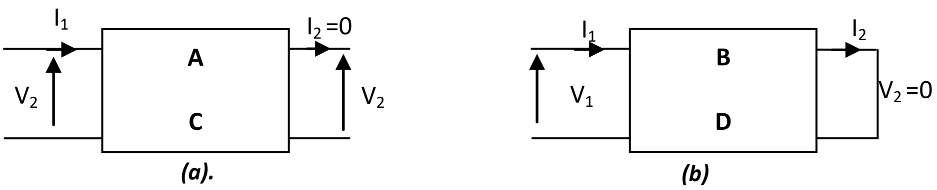


Figure 2-11 : Determination of the T parameters: (a)finding A and C, (b) finding B and D.

Table 2-5 : The value of ABCD Parameters

$A = \left(\frac{V_1}{V_2}\right)_{I_2=0}$	open – circuit Voltage ratio	dimensionless
$B = \left(-\frac{V_1}{I_2}\right)_{V_2=0}$	Negative Short-circuit transfer impedance	$[\Omega]$
$C_{21} = \left(\frac{I_2}{V_2}\right)_{I_2=0}$	open – circuit transfer admittance	$[\Omega^{-1}]$
$D = \left(-\frac{I_1}{I_2}\right)_{V_2=0}$	Negative short-circuit current ratio	dimensionless

Note:

Equations (2.9) and (2.10) link the input variables (I_1 and V_1) to the output variables (V_2 and $-I_2$), Notice that in computing the transmission parameters, $-I_2$ is used rather than I_2 because the current is considered to be leaving the network, as shown in Fig 2-10 In this context, I_2 is defined as the current leaving the network, as illustrated in figure. 2-1, This is done merely for conventional reasons; when you cascade two-ports (output to input), it is most logical to think of I_2 as leaving the two-port. It is also cus tomary in the power industry to consider I_2 as leaving the two-port.

Our last set of parameters may be defined by expressing the variables at the output port in terms of the variables at the input port. We obtain

$$V_2 = aV_1 - bI_1$$
$$I_2 = cV_1 - dI_1 \qquad (2.11)$$

In matrix form as:

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} \qquad (2.12)$$

The values of the parameters can be determined by setting V_1 (ouput port short-circuited) or I_O (output port open-circuited) Table 2-6.

Table 2-6 : The value of abcd Parameters (inverse transmission)

$a = \left(\frac{V_2}{V_1}\right)_{I_1=0}$	open – circuit Voltage ratio	dimensionless
$b = \left(-\frac{V_2}{I_1}\right)_{V_1=0}$	Negative Short-circuit transfer impedance	$[\Omega]$
$c = \left(\frac{I_2}{V_1}\right)_{I_1=0}$	open – circuit transfer admittance	$[\Omega^{-1}]$
$d = \left(-\frac{I_2}{I_1}\right)_{V_1=0}$	Negative short-circuit current ratio	dimensionless

2.4 Relationships Between Parameters

As a first example, let us determine the Z parameters from the H parameters.

From Eq. (2.1),

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \qquad (2.13.a)$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \qquad (2.13.b)$$

Also, from Eq. (2.5),

$$V_2 = H_{11}I_1 + H_{12}V_2 \qquad (2.14.a)$$

$$I_2 = H_{21}I_1 + H_{22}V_2 \qquad (2.14.a)$$

From Eq. (2.13.a),

$$Z_{11} = \left(\frac{V_2}{I_2}\right)_{I_2=0} \qquad (2.15.a)$$

From Eq. (2.14.b),

$$0 = H_{21}I_I + H_{22}V_O \qquad (2.16.a)$$

$$H_{21}I_I = -H_{22}V_O \qquad (2.16.b)$$

$$V_2 = \frac{H_{21}I_1}{H_{22}} \qquad (2.17)$$

$$V_1 = \left(H_{11} - \frac{H_{21}}{H_{22}}H_{12}\right)I_1 \qquad (2.18)$$

$$\frac{V_1}{I_1} = \left(\frac{H_{11}H_{22} - H_{21}H_{12}}{H_{22}}\right) = \frac{\Delta H}{H_{22}} \qquad (2.19)$$

$$Z_{11} = \frac{\Delta H}{H_{22}} \qquad (2.20)$$

From Eq. (2.13.a),

$$Z_{12} = \left(\frac{V_1}{I_2}\right)_{I_1=0} \qquad (2.21)$$

From Eq. (2.14.b),

$$V_1 = H_{12}V_2 \qquad (2.22)$$

$$I_2 = H_{22}V_2 \qquad (2.23)$$

$$Z_{12} = \frac{H_{12}}{H_{22}} \qquad (2.24.)$$

From Eq. (2.13.a),

$$Z_{21} = \left(\frac{V_2}{I_1}\right)_{I_2=0} \qquad (2.25)$$

From Eq. (2.14.b),

$$0 = H_{21}I_1 + H_{22}V_2 \qquad (2.26)$$

$$H_{21}I_1 = -H_{22}V_2 \qquad (2.27)$$

$$Z_{21} = -\frac{H_{21}}{H_{22}} \qquad (2.28)$$

From Eq. (2.13.b),

$$Z_{22} = \left(\frac{V_2}{I_2}\right)_{I_1=0} \quad (2.29)$$

From Eq. (2.14.b),

$$I_2 = H_{22}V_2 \quad (2.30)$$

$$Z_{22} = -\frac{1}{H_{22}} \quad (2.31)$$

2.3 Interrelation of parameters

Similarly all parameters can be related as shown in Table 2-7

Table 2-7 : Two-port parameter conversion table

Disered parameters	**ABCD**	**Z**	**Y**	H
ABCD	$\begin{bmatrix} A & B \\ C & D \end{bmatrix}$	$\begin{bmatrix} \frac{Z_{11}}{Z_{21}} & \frac{\Delta Z}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{bmatrix}$	$\begin{bmatrix} \frac{Y_{22}}{Y_{21}} & \frac{1}{Y_{21}} \\ \frac{\Delta Y}{Y_{21}} & \frac{Y_{11}}{Y_{21}} \end{bmatrix}$	$\begin{bmatrix} -\frac{\Delta H}{H_{21}} & -\frac{H_{11}}{H_{21}} \\ -\frac{H_{22}}{H_{21}} & -\frac{1}{H_{21}} \end{bmatrix}$
Z	$\begin{bmatrix} \frac{A}{C} & \frac{\Delta T}{C} \\ \frac{1}{C} & \frac{D}{C} \end{bmatrix}$	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} \frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\ -\frac{Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{bmatrix}$	$\begin{bmatrix} \frac{\Delta H}{H_{22}} & \frac{H_{12}}{H_{22}} \\ \frac{H_{21}}{H_{22}} & \frac{1}{H_{22}} \end{bmatrix}$
Y	$\begin{bmatrix} \frac{D}{B} & -\frac{\Delta T}{B} \\ -\frac{1}{B} & \frac{A}{B} \end{bmatrix}$	$\begin{bmatrix} \frac{Z_{22}}{\Delta Z} & -\frac{Z_{12}}{\Delta Z} \\ -\frac{Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{H_{11}} & -\frac{H_{12}}{H_{11}} \\ \frac{H_{21}}{H_{11}} & \frac{\Delta H}{H_{11}} \end{bmatrix}$
H	$\begin{bmatrix} \frac{B}{D} & -\frac{\Delta T}{D} \\ -\frac{1}{D} & \frac{C}{D} \end{bmatrix}$	$\begin{bmatrix} \frac{\Delta Z}{Z_{22}} & \frac{Z_{12}}{Z_{22}} \\ -\frac{Z_{21}}{Z_{22}} & \frac{1}{Z_{22}} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{Y_{11}} & -\frac{Y_{12}}{Y_{11}} \\ \frac{Y_{21}}{Y_{11}} & \frac{\Delta Z}{Y_{11}} \end{bmatrix}$	$\begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}$

$\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}$ $\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21}$ $\Delta H = H_{11}H_{22} - H_{12}H_{21}$
$\Delta T = AB - CD$

2.4 Condition for reciprocity

If the ratio of voltage at one port to the current at other port is same to the ratio if the positions of voltage and current are interchanged, then the network is said to be Condition for

Reciprocal Two-Port Network. The transfer impedances can be measured as shown in figure - 2.12 (a) and (b).

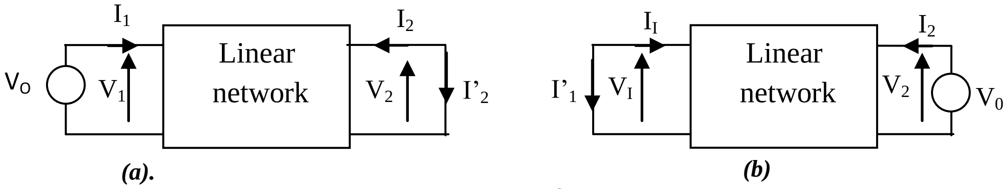


Figure 2-12 : Condition for reciprocity

$$\left(\frac{V_O}{I_2^{'}}\right)_{V_2=0} = \left(\frac{V_O}{I_1^{'}}\right)_{V_1=0} \tag{2.32}$$

$$\left(\frac{V_O}{I_2^{'}}\right)_{V_2=0} \tag{2.33}$$

In terms of Z Parameters

From Eq. (2.1),

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \tag{2.34.a}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \tag{2.34.b}$$

$$V_1 = V_O;\ I_2 = -I_2^{'}\ \ and\ \ V_2 = 0 \tag{2.35}$$

From Eq. (2.34.a),

$$0 = Z_{11}I_1 - Z_{12}I_2 \tag{2.36}$$

$$0 = Z_{21}I_1 - Z_{22}I_2^{'} \Rightarrow I_1 = -\frac{Z_{22}}{Z_{21}}I_2^{'} \tag{2.37}$$

$$V_O = \left(Z_{11}\frac{Z_{22}}{Z_{21}} - Z_{12}\right)I_2^{'} = \left(\frac{Z_{11}Z_{22} - Z_{21}Z_{12}}{Z_{21}}\right)I_2^{'} = \frac{Z}{Z_{21}}I_2^{'} \tag{.2.38}$$

$$\frac{V_O}{I_2^{'}} = \frac{Z}{Z_{21}} \tag{2.39}$$

$$V_2 = V_O;\ I_1 = -I_1^{'}\ \ and\ \ V_1 = 0 \tag{2.41}$$

$$\left(\frac{V_O}{I_1^{'}}\right)_{V_1=0} \tag{2.40}$$

From Eq. (2.34.b),

$$V_O = -Z_{21} I_1^{'} + Z_{22} I_2 \tag{2.42}$$

$$0 = -Z_{11} I_1^{'} + Z_{12} I_2 \Rightarrow I_2 = -\frac{Z_{11}}{Z_{12}} I_1^{'} \tag{2.43}$$

$$V_O = \left(-Z_{21} - Z_{22} \frac{Z_{11}}{Z_{12}} \right) I_1^{'} = \left(\frac{Z_{11} Z_{22} - Z_{21} Z_{12}}{Z_{12}} \right) I_1^{'} = \frac{Z}{Z_{12}} I_1^{'} \tag{2.44}$$

$$\frac{V_O}{I_1^{'}} = \frac{Z}{Z_{12}} \tag{2.45}$$

$$\left(\frac{V_O}{I_2^{'}} \right)_{V_2 = 0} = \left(\frac{V_O}{I_1^{'}} \right)_{V_1 = 0} \tag{2.46}$$

$$\frac{Z}{Z_{21}} = \frac{Z}{Z_{12}} \Rightarrow Z_{12} = Z_{21} \tag{2.47}$$

Conditions for Reciprocity and symmetry for Two-Port Networks in terms of the various parameters

Table 2-8 : Reciprocal And symmetry of Two-Port Circuits

Parametres	**Conditions for Reciprocity**	**Conditions for symmetry**
Z	$Z_{12}= Z_{21}$	$Z_{11}= Z_{22}$
Y	$Y_{12}= Y_{21}$	$Y_{11}= Y_{22}$
H	$H_{12}= -H_{21}$	$\Delta H = 1$
ABCD	AD-BC=1	A=D

2.5 Interconnection of Two-Port Networks

Two-port circuits may be interconnected in five ways :

- ✓ Series-series connection
- ✓ Parallel-parallel connection
- ✓ Series-parallel connection
- ✓ Parallel-series connection
- ✓ Cascade connection

2.5.1 Series-Series connection

When two-ports are connected in a series-series configuration as shown in Figure 2-13. the best choice of two-port parameter is **the *Z*-parameters**. The *y*-parameters of the combined network are found by matrix addition of the two individual *Z*-parameter matrices.

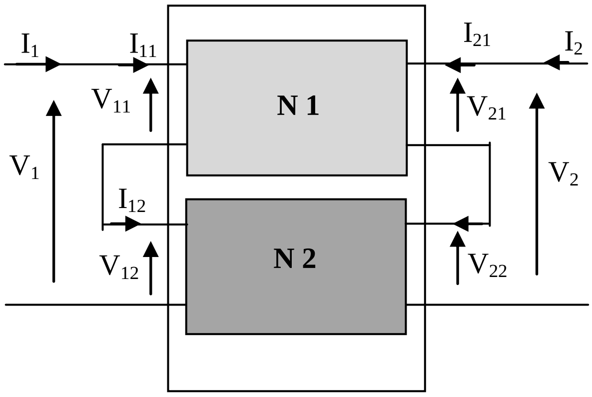


Figure 2-13 : Series-Series connection

Form network 1

$$\begin{aligned} V_{11} &= (Z_{11})_1 I_{11} + (Z_{12})_1 I_{21} \\ V_{21} &= (Z_{21})_1 I_{11} + (Z_{22})_1 I_{21} \end{aligned} \qquad (2.48)$$

And for network 2

$$\begin{aligned} V_{12} &= (Z_{11})_2 I_{12} + (Z_{12})_2 I_{22} \\ V_{22} &= (Z_{21})_2 I_{12} + (Z_{22})_1 I_{22} \end{aligned} \qquad (2.49)$$

We notice from figure 2-13 that

$$I_1 = I_{11} = I_{12} \qquad (2.50)$$

$$I_2 = I_{21} = I_{22} \qquad (2.51)$$

and that

$$\begin{aligned} V_1 &= V_{11} + V_{12} = [(Z_{11})_1 + (Z_{11})_2] I_{11} + [(Z_{12})_1 + (Z_{12})_2] I_{21} \\ V_2 &= V_{21} + V_{22} = [(Z_{21})_1 + (Z_{21})_2] I_{11} + [(Z_{22})_1 + (Z_{22})_2] I_{21} \end{aligned} \qquad (2.52)$$

Thus, the zparameters for the overall network are

$$\begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} = \begin{pmatrix} (Z_{11})_1 + (Z_{11})_2 & (Z_{12})_1 + (Z_{12})_2 \\ (Z_{21})_1 + (Z_{21})_2 & (Z_{22})_1 + (Z_{22})_2 \end{pmatrix} \qquad (2.53)$$

or

$$[Z] = [Z]_1 + [Z]_2 \qquad (2.54)$$

2.5.2 Parallel-parallel connection

When two-ports are connected in a parallel-parallel configuration as shown in Figure 2-14, the best choice of two-port parameter is **the *y*-parameters**. The *y*-parameters of the combined network are found by matrix addition of the two individual *y*-parameter matrices.

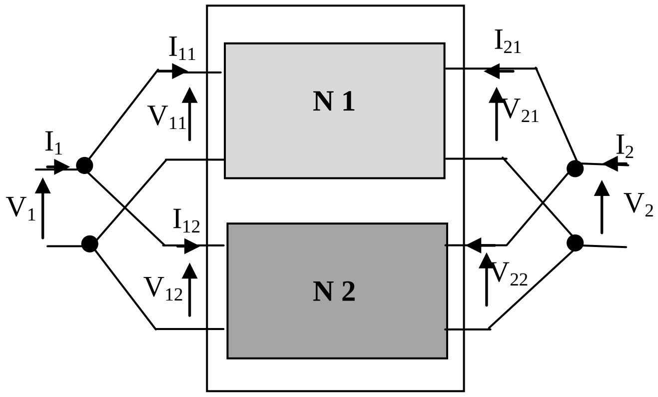


Figure 2-14 : Parallel-parallel connection

Form network 1

$$I_{11} = (Y_{11})_1 V_{11} + (Y_{12})_1 V_{21}$$
$$I_{21} = (Y_{21})_1 V_{11} + (Y_{22})_1 V_{21} \qquad (2.55)$$

Form network 2

$$I_{12} = (Y_{11})_2 V_{12} + (Y_{12})_2 V_{22}$$
$$I_{22} = (Y_{21})_2 V_{12} + (Y_{22})_1 V_{22} \qquad (2.56)$$

We notice from Figure 2-14 that

$$V_1 = V_{11} = V_{12}\,;\; V_2 = V_{21} = V_{22} \qquad (2.57)$$

$$I_1 = I_{11} + I_{12}\,;\; I_2 = I_{21} + I_{22} \qquad (2.58)$$

and that

$$I_1 = [(Y_{11})_1 + (Y_{11})_2]V_1 + [(Y_{12})_1 + (Y_{12})_2]V_2$$
$$I_2 = [(Y_{21})_1 + (Y_{21})_2]V_1 + [(Y_{22})_1 + (Y_{22})_2]V_2 \qquad (2.59)$$

Thus, the Y parameters for the overall network are

$$\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} = \begin{pmatrix} (Y_{11})_1 + (Y_{11})_2 & (Y_{12})_1 + (Y_{12})_2 \\ (Y_{21})_1 + (Y_{21})_2 & (Y_{22})_1 + (Y_{22})_2 \end{pmatrix} \qquad (2.60)$$

or

$$[Y] = [Y]_1 + [Y]_2 \qquad (2.61)$$

2.5.3 Series-Parallel connection

When two-ports are connected in a series-parallel configuration as shown in Figure 2-15, the best choice of two-port parameter is **the h-parameters**. The *h*-parameters of the combined network are found by matrix addition of the two individual *h*-parameter matrices

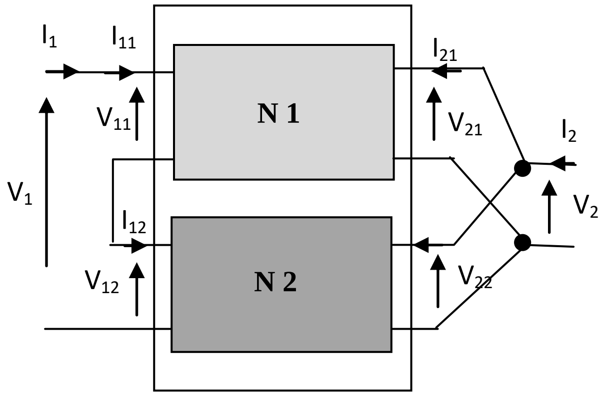


Figure 2-15 : Series-Parallel connection

Form network 1

$$V_{11} = (H_{11})_1 I_{11} + (H_{12})_1 V_{21}$$
$$I_{21} = (H_{21})_1 I_{11} + (H_{22})_1 V_{21} \quad (2.62)$$

Form network 2

$$V_{12} = (H_{11})_2 I_{12} + (H_{12})_2 V_{22}$$
$$I_{22} = (H_{21})_2 I_{12} + (H_{22})_1 V_{22} \quad (2.63)$$

We notice from Figure 2-15 that

$$V_1 = V_{11} + V_{12}\,;\; V_2 = V_{21} = V_{22} \quad (2.64)$$

$$I_1 = I_{11} = I_{12}\,;\; I_2 = I_{21} + I_{22} \quad (2.65)$$

and that

$$V_1 = [(H_{11})_1 + (H_{11})_2] I_1 + [(H_{12})_1 + (H_{12})_2] V_2$$
$$I_2 = [(H_{21})_1 + (H_{21})_2] I_1 + [(H_{22})_1 + (H_{22})_2] V_2 \quad (2.66)$$

Thus, the H parameters for the overall network are

$$\begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix} = \begin{pmatrix} (H_{11})_1 + (H_{11})_2 & (H_{12})_1 + (H_{12})_2 \\ (H_{21})_1 + (H_{21})_2 & (H_{22})_1 + (H_{22})_2 \end{pmatrix} \quad (2.67)$$

or

$$[H] = [H]_1 + [H]_2 \quad (2.68)$$

2.5.4 Parallel-Series connection

When two-ports are connected in a parallel-series configuration as shown in Figure 2-16, the best choice of two-port parameter is **the *g*-parameters**. The *g*-parameters of the combined network are found by matrix addition of the two individual *g*-parameter matrices

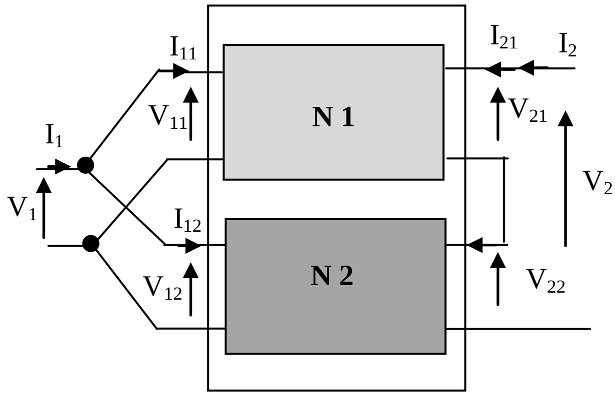


Figure 2-16 : Parallel-Series connection

Form network 1

$$I_{11}=(G_{11})_1V_{11}+(G_{12})_1I_{21}$$
$$V_{21}=(G_{21})_1V_{11}+(G_{22})_1I_{21} \tag{2.69}$$

Form network 2

$$I_{12}=(G_{11})_2V_{12}+(G_{12})_2I_{22}$$
$$V_{22}=(G_{21})_2V_{12}+(G_{22})_1I_{22} \tag{2.70}$$

We notice from Figure 2-16 that

$$V_1=V_{11}=V_{12}\,;\;V_2=V_{21}+V_{22} \tag{2.71}$$

$$I_1=I_{11}+I_{12}\,;\;I_2=I_{21}=I_{22} \tag{2.72}$$

and that

$$I_1=[(G_{11})_1+(G_{11})_2]V_1+[(G_{12})_1+(G_{12})_2]I_2$$
$$V_2=[(G_{21})_1+(G_{21})_2]V_1+[(G_{22})_1+(G_{22})_2]I_2 \tag{2.73}$$

Thus, the G parameters for the overall network are

$$\begin{pmatrix}G_{11} & G_{12}\\ G_{21} & G_{22}\end{pmatrix}=\begin{pmatrix}(G_{11})_1+(G_{11})_2 & (G_{12})_1+(G_{12})_2\\ (G_{21})_1+(G_{21})_2 & (G_{22})_1+(G_{22})_2\end{pmatrix} \tag{2.74}$$

or

$$[G]=[G]_1+[G]_2 \tag{2.75}$$

2.5.5 Cascade connection

When two-ports are connected with the output port of the first connected to the input port of the second (a cascade connection) as shown in Figure 2-17, the best choice of two-port parameter is the ***ABCD*-parameters**. The *a*-parameters of the combined network are found by matrix multiplication of the two individual *a*-parameter matrices

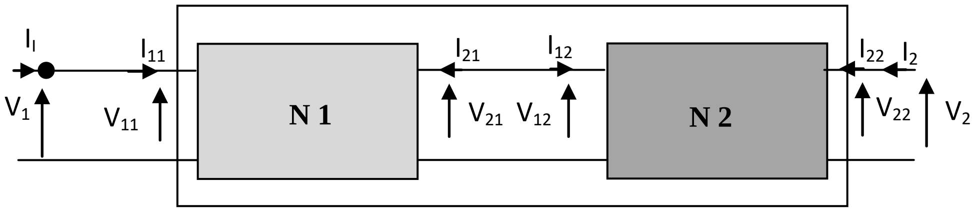


Figure 2-17 : Cascade connection

The transmission parameters can be obtained by simple matrix multiplication:
For the two networks,
Form network 1

$$\begin{pmatrix} V_{21} \\ V_{21} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_{11} \\ -I_{11} \end{pmatrix} \tag{2.76}$$

Form network 2

$$\begin{pmatrix} V_{22} \\ I_{22} \end{pmatrix} = \begin{pmatrix} A' & B' \\ C' & D' \end{pmatrix} \begin{pmatrix} V_{12} \\ -I_{12} \end{pmatrix} \tag{2.77}$$

From Figure 2-17,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} V_{11} \\ I_{11} \end{bmatrix}, \quad \begin{bmatrix} V_{21} \\ -I_{21} \end{bmatrix} = \begin{bmatrix} V_{12} \\ I_{12} \end{bmatrix}, \quad \begin{bmatrix} V_{22} \\ -I_{22} \end{bmatrix} = \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{2.78}$$

Substituting these into Eqs. (2.71) and (2.72),

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \times \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} \begin{bmatrix} V_1 \\ -I_1 \end{bmatrix} \tag{2.79}$$

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} AA' + BC' & AB' + BD' \\ CA' + DC' & CB' + DD' \end{bmatrix} \begin{bmatrix} V \\ -I_1 \end{bmatrix} \tag{2.80}$$

or

$$[T] = [T]_1 \times [T]_2 \tag{2.81}$$

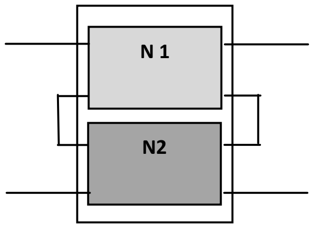
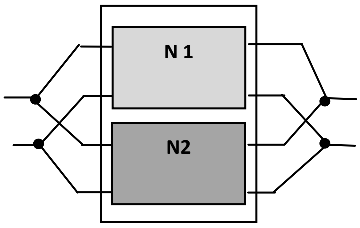
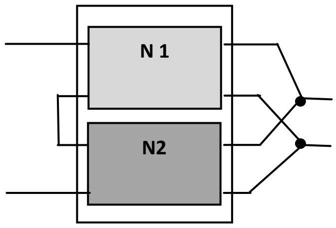
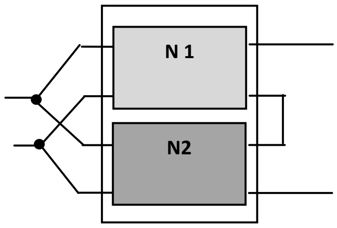
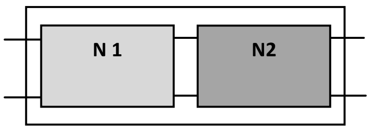
For n=1 to N Q's connected in cascade:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \prod_{n=1} T_n \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{2.82}$$

2.5.6 Summary of the interconnection of Two Port Network

Similarly all interconnection of Two Port Network as shown in Table 2-9

Table 2-9 : Summary of the interconnection of Two Port Networks

	Parametres	
S-S connection		$[Z]=[Z]_1+[Z]_2$
P-P connection		$[Y]=[Y]_1+[Y]_2$
S-P connection		$[H]=[H]_1+[H]_2$
P-S connection		$[G]=[G]_1+[G]_2$
Cascade connection		$[T]=[T]_1\times[T]_2$

2.6 Characteristics of Terminated Two-Ports

Four characteristics of a terminated two-port circuit define its terminal behavior:

- ✓ The Input Impedance
- ✓ The current gain
- ✓ The voltage gain
- ✓ The output Impedance

2.6.1 Characteristics in terms of z Parameters

We derive the 4 characteristics in terms of z parameters**.**

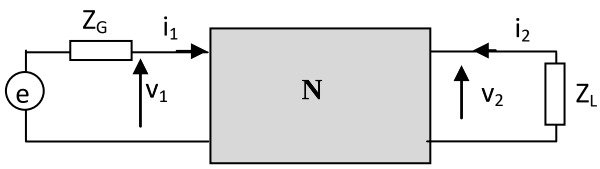


Figure 2-18 : Loaded two- port

Recall the circuit relation for the Z parameters:

$$V_1 = Z_{11} I_1 + Z_{12} I_2$$
$$V_2 = Z_{21} I_2 + Z_{22} I_2 \qquad (2.83)$$

Connection with the source and termination with the load imposes the following equations:

$$V_2 = -Z_L I_2 \qquad (2.84)$$

$$V_1 = V_1 + Z_G I_1 \qquad (2.85)$$

The characteristics are obtained by using the equations relevant for the computation

2.6.2 The Input Impedance

In order to obtain the input impedance, we first obtain port-2 current in terms of port-1 current:

$$Z_I = \frac{V_1}{I_1} \qquad (2.86)$$

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \qquad (2.87.a)$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 = -Z_L I_2 \qquad (2.87.b)$$

$$Z_{21} I_1 + Z_{22} I_2 = -Z_L I_2 \Rightarrow -(Z_L + Z_{22}) I_2 = Z_{21} I_1 \qquad (2.88)$$

$$I_2 = -\frac{Z_{21}}{Z_L + Z_{22}} I_1 \tag{2..89}$$

We then use this in the equation for port-1 voltage

$$V_1 = \left(Z_{11} + \frac{Z_{12}Z_{21}}{Z_L + Z_{22}} \right) I_1 \tag{2.90}$$

In this fashion, we obtain the input impedance as:

$$Z_I = \frac{V_1}{I_1} = \left(Z_{11} + \frac{Z_{12}Z_{21}}{Z_L + Z_{22}} \right) \tag{2.91}$$

2.6.3 The Current Gain

$$\mathrm{G}_I = \frac{I_2}{I_1} \tag{2.92}$$

The current gain is easily found from

$$Z_{21}I_1 + Z_{22}I_2 = -Z_L I_2 \Rightarrow -(Z_{22} + Z_L)I_2 = Z_{21}I_1 \tag{2.93}$$

$$\mathrm{G}_I = \frac{I_2}{I_1} = -\frac{Z_{21}}{Z_{22} + Z_L} \tag{2.94}$$

2.6.4 The Voltage Gain

$$\mathrm{G}_V = \frac{V_2}{V_1} \tag{2.95}$$

To find the voltage gain, we recall that:

$$V_1 = Z_I I_1 = \left(Z_{11} + \frac{Z_{12}Z_{21}}{Z_L + Z_{22}} \right) I_1 \text{ and } \mathrm{V}_2 = -Z_L I_2 \tag{2.96}$$

Using the current gain derived above, we find:

$$\mathrm{G}_V = \frac{V_2}{V_1} = \frac{-Z_L I_2}{Z_I I_1} = \frac{-Z_L}{Z_{11} - \frac{Z_{12}Z_{21}}{Z_L + Z_{22}}} \frac{Z_{21}}{Z_{22} + Z_L} \tag{2.97}$$

$$= \frac{Z_L Z_{21}}{\left(\frac{Z_{11}Z_L + Z_{11}Z_{22} - Z_{12}Z_{21}}{Z_L + Z_{22}} \right) Z_{22} + Z_L} \tag{2.98}$$

$$\mathrm{G}_V = \frac{Z_L Z_{21}}{Z_{11}Z_L + Z_{11}Z_{22} - Z_{12}Z_{21}} = \frac{Z_L Z_{21}}{Z_{11}Z_L + \Delta Z} \tag{2.99}$$

2.6.5 Thevenin Parameters seen from Port-2

Thevenin impedance is found by setting the source voltage to zero finding the ratio

$$Z_O = \frac{V_2}{I_2} \quad (2.100)$$

$$Z_{11}I_1 + Z_{12}I_2 = 0 - Z_g I_1 \Rightarrow (Z_{11} + Z_g)I_1 = Z_{12}I_2 \quad (2.101)$$

$$-(Z_{11} + Z_g)I_1 = Z_{12}I_2 \Rightarrow I_1 = -\frac{Z_{12}}{Z_{11} + Z_g} I_2 \quad (2.102)$$

$$V_2 = \left(\frac{Z_{21}Z_{12}}{Z_{11} + Z_g} + Z_{22}\right) I_2 \quad (2.103)$$

The Thevenin impedance is hence obtained as:

$$Z_o = \frac{V_2}{I_2} = \left(\frac{Z_{21}Z_{12}}{Z_{11} + Z_g} + Z_{22}\right) \quad (2.104)$$

2.7 What is a Filter?

A filter is a circuit designed to allow signals with desired frequencies to pass through while rejecting or attenuating others.

2.8 Types of Electrical Filters

- **Passive filters** are composed of only passive components (resistors, capacitors, inductors) and do not provide amplification
- **Active filters** is a filter consists of active elements (such as transistors and op-amps) in addition to passive elements *R*, *L*, and *C*.

2.9 Passive Filters

2.9.1 Low-pass filter:

A **low-pass filter** passes low frequencies and stops high frequencies, as shown ideally in Figure 2-19

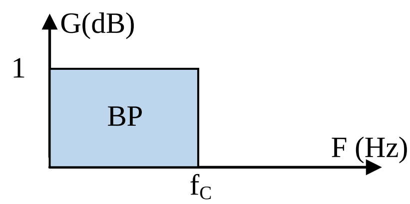


Figure 2-19 : Low-pass filter

2.9.2 High-pass filter

A **high-pass filter** passes high frequencies and rejects low frequencies, as shown ideally in Figure 2-20

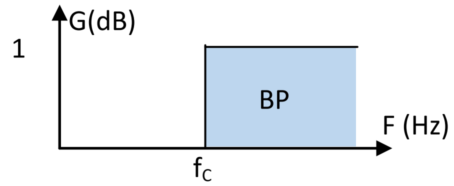


Figure 2-20 : High-pass filter

2.9.3 Band-pass filter

A **band-pass filter passes** frequencies within a frequency band and blocks or attenuates frequencies outside the band, as shown ideally in Figure 2-21

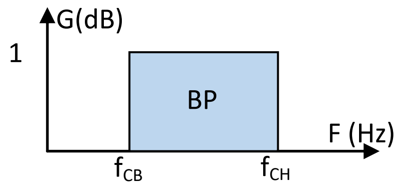


Figure 2-21 : Band-pass filter

2.9.4 Band-stop filter

A **band-stop filter** passes frequencies outside a frequency band and blocks or attenuates frequencies within the band, as shown ideally in Figure 2-22.

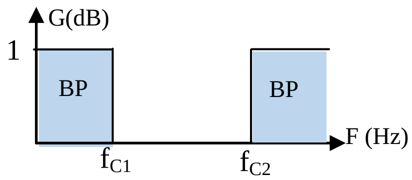


Figure 2-22 : Band-stop filter

2.10 Bode plot

A **Bode plot** is a graphical representation of a linear, time-invariant system's frequency response. It consists of two separate plots:

- ✓ **Magnitude Plot**: Shows how the amplitude of the system's output varies with frequency
- ✓ **Phase Plot**: Shows how the phase shift of the system's output varies with frequency.

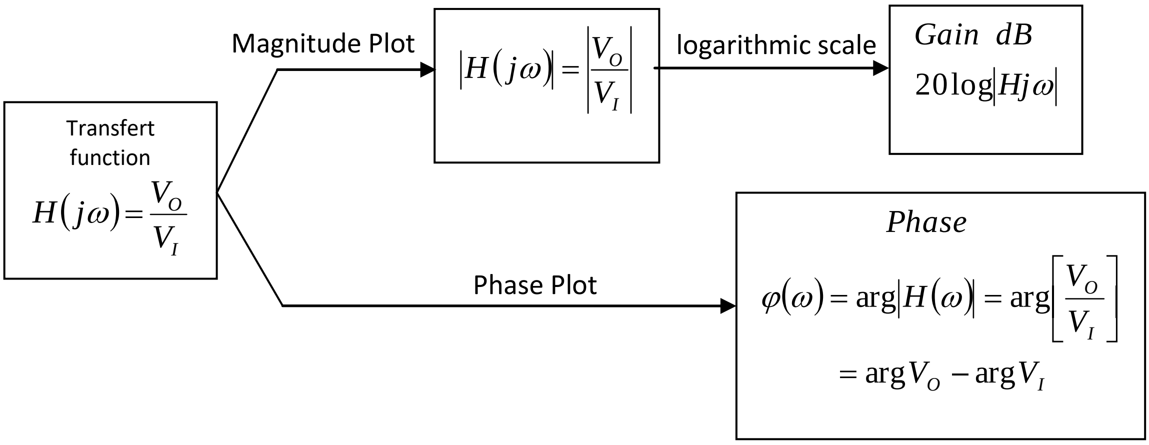


Figure 2-23 : Determination of gain and phase shift

2.11 Transfer Function

The transfer function of a circuit is the ratio of a phasor output Y(w) (an element voltage or current) to a phasor input X(w) (source voltage or current) that changes with frequency

$$H(j\omega)=\frac{Y(\omega)}{X(\omega)} \tag{2.105}$$

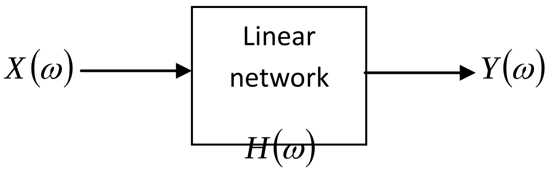


Figure 2-24 : A block diagram representation of a linear network

2.12 The Decible (d_B) :

The decibel (dB) is a logarithmic unit used to measure sound level. dB (decibel) is a logarithmic unit used to express the ratio between two values, typically power, intensity, or voltage

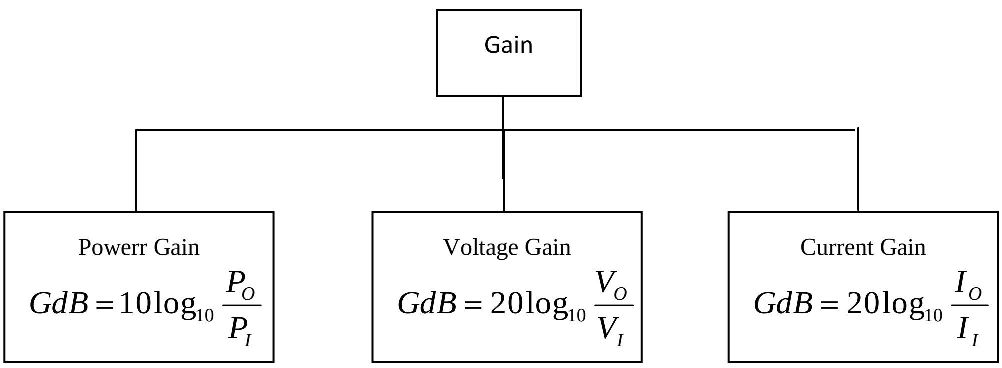


Figure 2-25 : Power gain Voltage gain and current gain

2.13 Importance of logarithmic scales:

Since the range of frequencies applied to electrical circuits is very wide, logarithmic scales are used when plotting transfer functions.

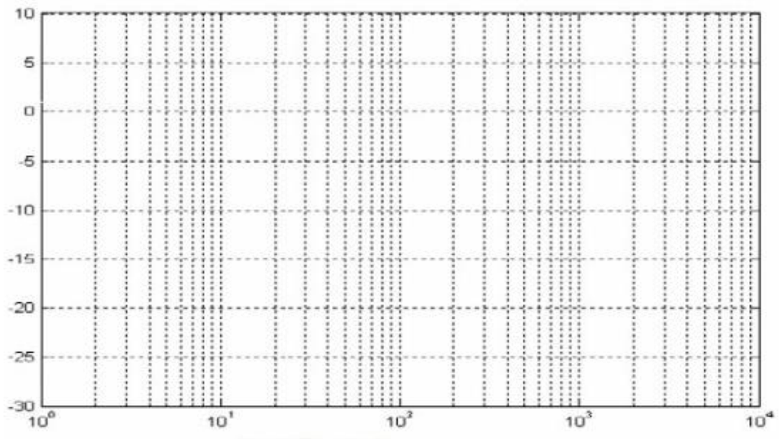
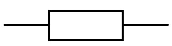
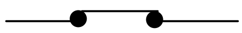
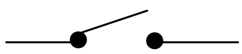
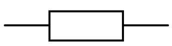
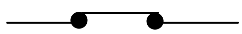


Figure 2-26 : logarithmic scales and Linear scale

2.14 Behavior of R L and C impedances as a function of frequency

Table 2-10 shows the Behavior of R L and C impedances as a function of frequency

Table 2-10 : Qualitative analysis of filters

	Resistor	**Capacitor**	**Condctor**
Impdance	$Z_R = R$	$Z_C = \dfrac{1}{jC\omega}$	$Z_L = jL\omega$
Impedance module	$\lvert Z_R \rvert = R$	$\lvert Z_C \rvert = \dfrac{1}{C\omega}$	$Z_L = L\omega$
High frequency	R	$\lim\limits_{\omega\to\infty} \lvert Z_C \rvert = \dfrac{1}{C\times\infty} = 0$	$\lim\limits_{\omega\to\infty} \lvert Z_L \rvert = +\infty$
Low frequency	R	$\lim\limits_{\omega\to 0} \lvert Z_C \rvert = \dfrac{1}{C\times 0} = +\infty$	$\lim\limits_{\omega\to 0} \lvert Z_L \rvert = L\times 0 = 0$
Equivanlent model (HF)			
Equivanlent model (HF)			

2.15 Cut-off frequency of a filter

Cut-off frequencies are the frequency limits of a filter's passband, they are defined by the following condition on the magnitudes:

$$H(f_c) = \frac{H_{Max}}{\sqrt{2}} \tag{2.106}$$

$$20\log G(f_c) = 20\log\frac{G_{Max}}{\sqrt{2}} = 20\log G_{Max} - 20\log\sqrt{2} = G_{Max} - 3dB \tag{2.107}$$

2.16 Low-pass RC filters

A typical lowpass filter is formed when the output of an RC circuit is taken off the capacitor as shown in Figure 2-27

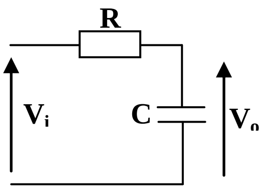
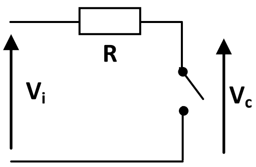
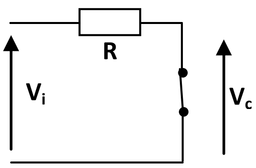


Figure 2-27: Low-pass RC filters circuit

- **Asymptotic behavior**

Table 2-11 shows the asympototic behavior of Low-pass RC filter

Table 2-11: Asymptotic behavior

	System diagrram	Study of the output Signal value	conlusion
Behavior at low frequencies		$V_C \neq 0V$	The system passes low frequecies
Behavior at high frequencies		$V_C = 0V$	The system cuts high frequencies

- **The transfer function**

By applying the voltage divider Rule, we can determine The transfer function

$$H(j\omega)=\frac{V_O}{V_I} \quad (2.108)$$

$$V_O=\frac{Z_C}{Z_C+Z_R}V_I \quad (2.109)$$

$$H(j\omega)=\frac{V_O}{V_I}=\frac{\frac{Z_C}{Z_C+Z_R}V_I}{V_I}=\frac{\frac{1}{jC\omega}}{R+\frac{1}{jC\omega}}=\frac{\frac{1}{jC\omega}}{\frac{jRC\omega+1}{jC\omega}} \quad (2.110)$$

$$H(j\omega)=\frac{1}{1+jRC\omega} \quad (2.111)$$

- **Cut-off pulse of a filter**

The cut-off pulse can be calculated as follows

$$H(\omega_c)=\frac{H_{Max}}{\sqrt{2}} \quad (2.112)$$

$$H_{Max}=H(\omega\to 0)=1\Rightarrow \frac{1}{\sqrt{1+R^2C^2\omega_0^2}}=\frac{1}{\sqrt{2}} \quad (2.113)$$

$$1+(RC\omega_C)^2=2 \quad (2.114)$$

$$RC\omega_C=1 \quad (2.115)$$

$$\omega_C=\frac{1}{RC} \quad (2.116)$$

a- Magnitude Plot

From Eq. (2.111),

$$H(j\omega)=\frac{1}{1+jRC\omega} \quad (2.117)$$

The magnitude of the transfer function (Gain) is:

$$|H(j\omega)|=\left|\frac{1}{1+jRC\omega}\right|=\frac{1}{\sqrt{1+(RC\omega)^2}}=\frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_C}\right)^2}} \quad (2.118)$$

$$|G(j\omega)|_{dB} = 20\log|H(j\omega)| = 20\log\left(\frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_C}\right)^2}}\right) = -10\log\left(1+\left(\frac{\omega}{\omega_C}\right)^2\right) \quad (2.119)$$

- **Phase Plot**

  The argument of the transfer function (Phase) is:

$$\varphi(\omega) = \arg[H(\omega)] = \arg\left[\frac{1}{1+j\frac{\omega}{\omega_0}}\right] = \arg[1] - \arg\left[1+j\frac{\omega}{\omega_0}\right] \quad (2.120)$$

$$\varphi(\omega) = arctg[0] - arctg\left[\frac{\omega}{\omega_0}\right] = -arctg\left[\frac{\omega}{\omega_0}\right] \quad (2.121)$$

Table 2-12 : Magnitude and pase reponse vs freuency for first-order loww-pass filter

ω	**0**	$\frac{\omega}{\omega_C}$	ω_C	$10\omega_C$	∞
$\|H(j\omega)\|$	1	-	$\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{10}}$	0
$\|G(j\omega)\|_{dB} = 20\log\|H(j\omega)\|$	0	-	-3dB	-20dB	$-\infty$
φ	0	-	$-\frac{\pi}{4}$	-	$-\frac{\pi}{2}$

Figure 2-28 shown the Bode plots for magnitude plot and phase plor

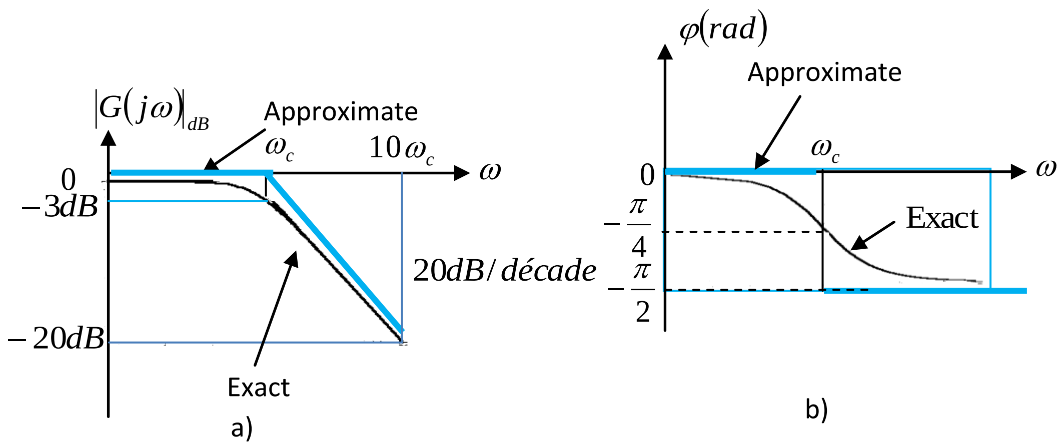


Figure 2-28 : Bode plots : (a) magnitude plot, (b) phase plot

These curves characterize a low-pass filter (the system attenuates high frequencies). The frequency band [0, w_c] is called the passband of the filter.

Note :

- **decade**
- **One decade** is a unit for measuring ratios on a logarithmic scale, with one decade corresponding to a ratio of 10 between two numbers.
- **octave**

One octave is a logarithmic unit for ratios between frequencies, with one octave corresponding to a doubling of frequency

2.17 High-pass Filters

A highpass filter is formed when the output of an RC circuit is taken off the resistor as shown in Figure 2-29

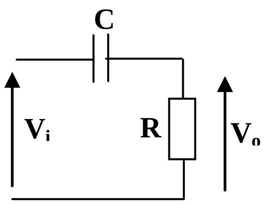
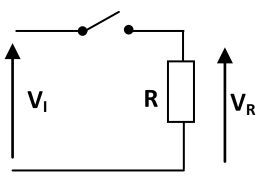
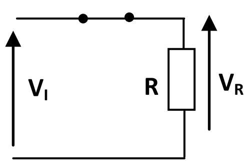


Figure 2-29 : High-pass filter

Table 2-10 shows the asympototic behavior of high-pass RC filter

Table 2-13: Asymptotic behavior

	System diagrram	Study of the output Signal value	conlussion
Behavior at low frequencies		$V_R = 0V$	The system cuts low frequecies
Behavior at high frequencies		$V_R \neq 0V$	The system passes high frequecies

a- The transfer function

By applying the voltage divider Rule, we can determine The transfer function

$$H(j\omega)=\frac{V_O}{V_I} \quad (2.122)$$

$$V_O=\frac{Z_R}{Z_C+Z_R}V_I \quad (2.123)$$

$$H(j\omega)=\frac{V_O}{V_I}=\frac{\frac{Z_R}{Z_C+Z_R}V_I}{V_I}=\frac{R}{\left(R+\frac{1}{jC\omega}\right)} \quad (2.124)$$

$$=\frac{R\left(\frac{1}{R}\right)}{\left(R+\frac{1}{jC\omega}\right)\left(\frac{1}{R}\right)}=\frac{1}{\left(1+\frac{1}{jRC\omega}\right)} \quad (2.125)$$

$$H(j\omega)=\frac{1}{\left(1-\frac{j}{RC\omega}\right)} \quad (2.126)$$

Cut-off pulse of a filter

The cut-off pulse

$$\omega_C=\frac{1}{RC} \quad (2.127)$$

Magnitude Plot

From Eq. (2.126), The magnitude of the transfer function (Gain) is:

$$|H(j\omega)|=\left|\frac{1}{1-\frac{j}{RC\omega}}\right|=\frac{1}{\sqrt{1+\left(\frac{1}{RC\omega}\right)^2}}=\frac{1}{\sqrt{1+\left(\frac{\omega_C}{\omega}\right)^2}} \quad (2.128)$$

$$|G(j\omega)|_{dB}=20\log|H(j\omega)|=20\log\left(\frac{1}{\sqrt{1+\left(\frac{\omega_C}{\omega}\right)^2}}\right)=-10\log\left(1+\left(\frac{\omega_C}{\omega}\right)^2\right) \quad (2.129)$$

b- Phase Plot

The argument of the transfer function (Phase) is:

$$\varphi(\omega)=\arg[H(\omega)]=\arg\left[\frac{1}{1-j\frac{\omega_0}{\omega}}\right]=\arg[1]-\arg\left[1-j\frac{\omega}{\omega_0}\right] \tag{2.130}$$

$$\varphi(\omega)=arctg[0]+arctg\left[\frac{\omega}{\omega_0}\right]=arctg\left[\frac{\omega}{\omega_0}\right] \tag{2.131}$$

Table 2-14 : Magnitude and pase reponse vs freuency for first-order high-pass filter

ω	**0**	$\frac{\omega}{\omega_C}$	ω_C	$10\omega_C$	∞
$\lvert H(j\omega)\rvert$	0	$\frac{1}{10}$	$\frac{1}{\sqrt{2}}$	-	1
$\lvert G(j\omega)\rvert_{dB}=20\log\lvert H(j\omega)\rvert$	$-\infty$	20dB	-3dB	-	0
φ	$\frac{\pi}{2}$	-	$\frac{\pi}{4}$	-	0

Figure 2-30 shown the Bode plots for magnitude plot and phase plot

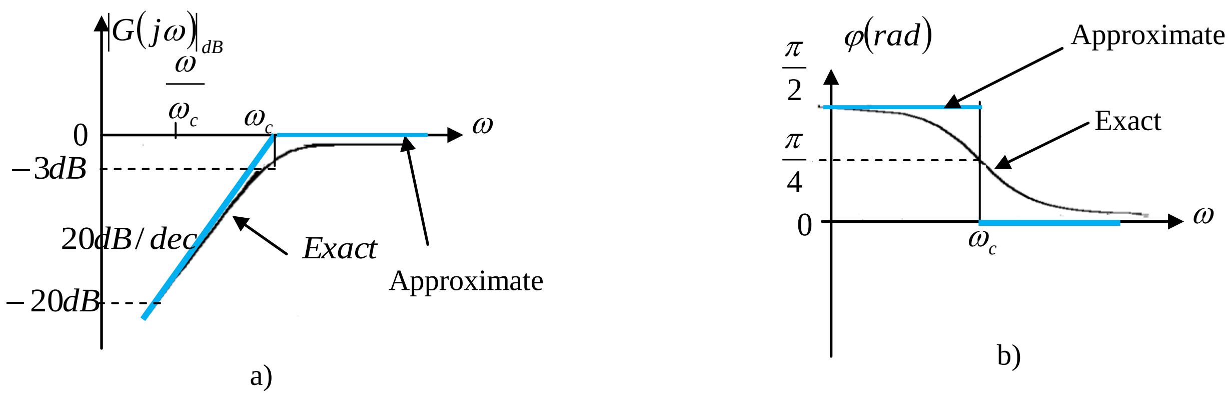


Figure 2-30 : Bode plots : (a) magnitude plot, (b) phase plot (haigh passfilter)

This curve characterizes a high-pass filter (the system attenuates low frequencies). The frequency band [ωc, ∞] is called the passband of the filter.

2.18 Glossary

Francais	English	العربية
Les quadripôles	Quadripole	رباعيات الاقطاب
Impédances	Impedance	الممانعة
Admittances	Admittance	المسامحة
Hybrides	Hybrid	الهجينة
Transmission	Transmission	التحويل
Les filtres	Filter	مرشح
Filtre passe bas	Low-pass filter	مرشح تمرير منخفض
Filtre passe haut	High-pass filter	مرشح تمريرة عالية
Filtre coupe bande	Band-stop filter	مرشح النطاق الترددي
Filtre passe bande	Band-pass filter	مرشح تمرير النطاق
La fréquence de coupure	The cut-off frequency	تواتر القطع

TWO-PORTE NETWORKS

Exercises

Exercise 2.1: Calculation of the impedance Matrix of a Two-Port Networks

Determine the impedance parameters of the T network
shown in Figure 2-31.

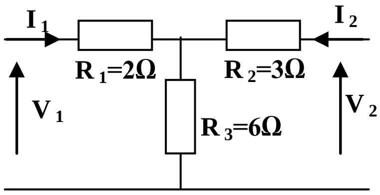


Figure 2-31 : Circuit for Exercise 02.1

Exercise 2.2 : Calculation of the Hybrid Matrix of a Two-Port Network

Determine the hybrid parameters of the T network
shown in Figure 2-31

Exercise 2.3 : Calculation of the impedance Matrix of a Two-Port Network from its transmission Matrix

Determine the impedance matrix (Z) of Two-Port networks, for a given matrix (ABCD)

Exercise 2.4 : Parallel-Parallel Association of Two-Port Networks

We consider the two-port network in Figure 2-32, composed of a T-network (with resistor R_1 and capacitor C) bridged by a resistor R_2

Demonstrate that this two-port network can be considered as the parallel association of two two-port networks, and draw the corresponding diagrams.

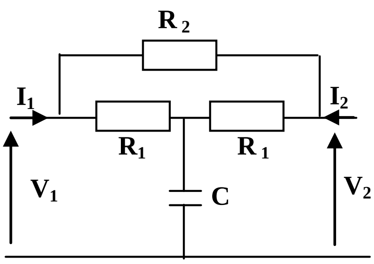


Figure 2-32 : Circuit for Exercise 02.4

Exercise 2.5: Determination of a Transfer Matrix by Cascade Decomposition

1- Calculate the transmission parameters of figure using the short-circuit and open-circuit method.

2- Figure 2-33 consists of a cascade association of two two-port networks, Q_1 and Q_2 (see dotted lines). Calculate the chain parameters for Q_1 and Q_2 . Deduce the chain parameters of the two-port network formed by the cascade association of these two two-port networks.

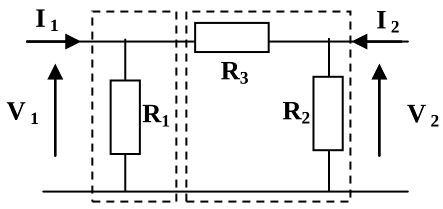


Figure 2-33 : Circuit for Exercise 02.5

Exercise 2. 6 : Low-Pass Filtre

a- Find the transfer function of the circuit in Figure 2-34 and express it in the specified form.

b- Plot the Bode diagram of this function.

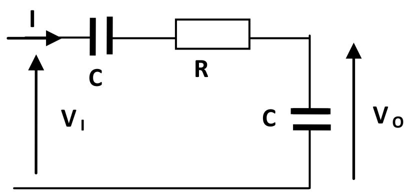


Figure 2-34 : Circuit for Exercise 02.34

TWO-PORT NETWORKS

Solutions

Exercise 2.1: Calculation of the impedance Matrix of a Two-Port Network

To find Z_{11} and Z_{21} , the output terminals are open circuited. Also connect a voltage source V_1 to the input terminals. This gives a circuit diagram as shown in Figure 2-31.a.

$$Z_{11} = \left(\frac{V_1}{I_1}\right)_{I_2=0} = ?$$

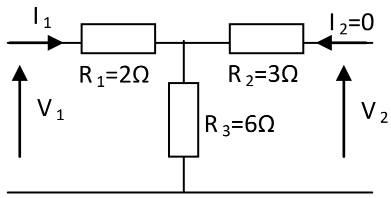


Figure 2-31.a

Applying KVL to the left-mesh, we get

$$V_1 = (R_1 + R_3)I_1$$

$$Z_{11} = \left(\frac{V_1}{I_1}\right)_{I_2=0} = \frac{(R_1 + R_3)I_1}{I_1} = R_1 + R_3 = 2 + 6 = 8\Omega$$

$$Z_{21} = \left(\frac{V_2}{I_1}\right)_{I_2=0} = ?$$

Applying KVL to the right-mesh, we get

$$V_2 = R_2 I_1$$

$$Z_{21} = \left(\frac{V_2}{I_1}\right)_{I_2=0} = \frac{R_2 I_1}{I_1} = R_2 = 6\Omega$$

To find Z_{12} and Z_{22} , the output terminals are open circuited. Also connect a voltage source V_2 to the input terminals. This gives a circuit diagram as shown in Figure 2-31.b.

$$Z_{12} = \left(\frac{V_1}{I_2}\right)_{I_1=0} = ?$$

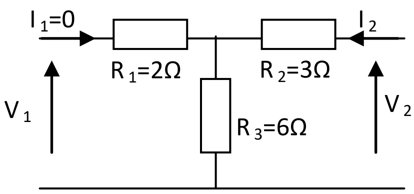


Figure 2-31.b

Applying KVL to the right-mesh, we get

$$V_1 = R_2 I_2$$

$$Z_{12} = \left(\frac{V_1}{I_2}\right)_{I_1=0} = \frac{R_2 I_2}{I_2} = R_2 = 6\Omega$$

$$Z_{22} = \left(\frac{V_2}{I_2}\right)_{I_1=0} = ?$$

Applying KVL to the left-mesh, we get

$$V_2 = (R_2 + R_3)I_1$$

$$Z_{22} = \left(\frac{V_2}{I_2}\right)_{I_1=0} = \frac{(R_2 + R_3)I_1}{I_1} = R_2 + R_3 = 6 + 3 = 9\Omega$$

It may be noted that, $Z_{12}=Z_{21}$. Thus, in matrix form we have

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 8 & 6 \\ 6 & 9 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Exercise 2.2: Calculation of the Hybrid Matrix of a Two-Port Network

To find H_{11} and H_{21} short-circuit the output terminals so that $V_2 = 0$. Also connect a current source I_1 to the input port as in Figure 2-31. c

$$H_{11} = \left(\frac{V_1}{I_1}\right)_{V_2=0} = ?$$

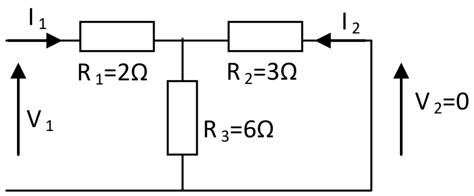


Figure 2-31.c

Referring to Figure 2-31.c, we find that

$$V_2 = \left(\frac{R_2 \times R_3}{R_2 + R_3} + R_1\right)I_1$$

$$H_{11} = \left(\frac{V_1}{I_1}\right)_{V_2=0} = \frac{\left(\frac{R_2 \times R_3}{R_2 + R_3} + R_1\right)I_1}{I_1} = \frac{R_2 \times R_3}{R_2 + R_3} + R_1 = \frac{3 \times 6}{3 + 6} + 2 = 4\Omega$$

$$H_{21} = \left(\frac{I_1}{I_2}\right)_{V_2=0} = ?$$

By using the principle of current division, we find that

$$I_2 = -\frac{R_3}{R_2 + R_3} I_1 = -\frac{6}{6 + 3} I_1$$

$$H_{21} = \left(\frac{I_2}{I_1}\right)_{V_2=0} = -\frac{\frac{6}{6+3}I_1}{I_1} = \frac{6}{6+3} = \frac{6}{9} = \frac{2}{3}$$

To obtain H_{12} and H_{22}, open-circuit the input port and connect a voltage source V_2 to the output port as in Figure 2-31.d

$$H_{12} = \left(\frac{V_1}{V_2}\right)_{I_1=0} = ?$$

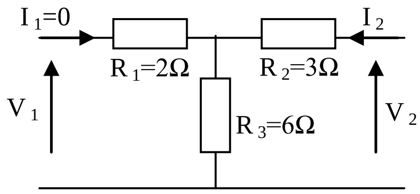


Figure 2-31. d

Using the principle of voltage division,

$$V_1 = \frac{R_3}{R_2+R_3}V_2 = \frac{6}{6+3}V_2$$

$$H_{12} = \left(\frac{V_1}{V_2}\right)_{I_1=0} = \frac{\frac{6}{6+3}V_2}{V_2} = \frac{6}{6+3} = \frac{2}{3}$$

Also,

$$H_{12} = \left(\frac{I_2}{V_2}\right)_{I_1=0} = ?$$

$$V_2 = (R_2+R_3)I_2$$

$$H_{12} = \left(\frac{I_2}{V_2}\right)_{I_1=0} = \frac{I_2}{(R_2+R_3)I_2} = \frac{1}{(R_2+R_3)} = \frac{1}{(6+3)} = \frac{1}{9}S$$

It may be noted that,H_{12}=-H_{21}.Thus,in matrix form we have

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 4 & \frac{2}{3} \\ -\frac{2}{3} & \frac{1}{9}S \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Exercise 2.3: Calculation of the impedance Matrix of a Two-Port Network from its transmission Matrix

Us proceed to find z parameters in terms of ABCD parameters. The ABCD parameters of a two-port network are defined by

$$V_I = AV_O - BI_O$$
$$I_I = CV_O - DI_O$$

$$\Rightarrow V_O = \frac{1}{C}(I_I + DI_O)$$

$$\Rightarrow V_O = \frac{I_I}{C} + \frac{D}{C}I_O \qquad (A)\ V_I = A\left(\frac{I_I}{C} + \frac{D}{C}I_O\right) - BI_O$$

$$V_I = A\frac{I_I}{C} + \left(\frac{AD}{C} - B\right)I_O \qquad (B)$$

Comparing equations A and B with

$$V_i = Z_{11}I_i + Z_{12}I_o$$
$$V_o = Z_{21}I_I + Z_{22}I_o$$

respectively, we find that

$$Z_{11} = \frac{A}{C},\quad Z_{12} = \frac{AD-BC}{C},\quad Z_{21} = \frac{1}{C} \quad and \quad Z_{22} = \frac{D}{C}$$

Exercise 2.4: Parallel-Parallel Association of Two-Port Networks

Figure 2-32.a show the Parallel-Parallel Association of Two-Port Networks

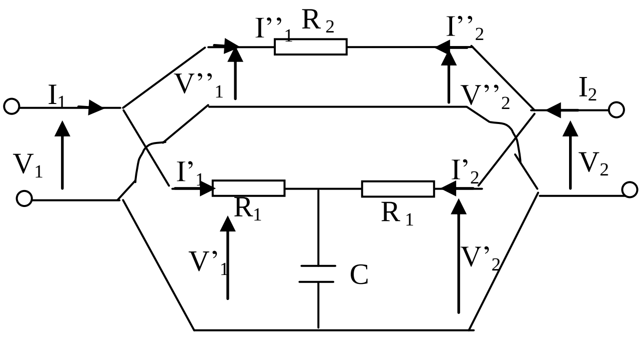


Figure 2-32.a

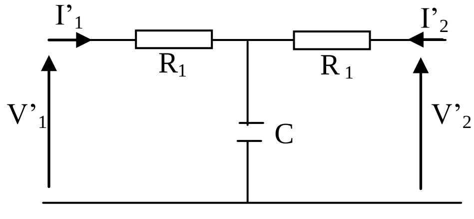


Figure 2-32.b: T-network

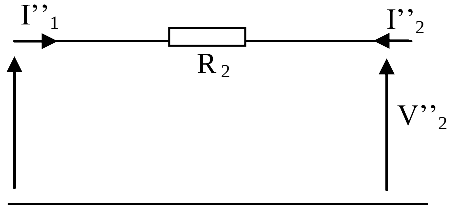


Figure 2-32.c: Bridged

Form Eq. (2.3)

$$\begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}I_2 \end{cases} \qquad (A)$$

$$[Y] = [Y^{'}] + [Y^{''}]$$

T nertwork

For this two-port network, which is passive and symmetric, we can write:

$$\begin{cases} I'_1 = Y'_{11}V'_1 + Y'_{12}V'_2 \\ I'_2 = Y'_{21}V'_1 + Y'_{22}V'_2 \end{cases} \qquad \begin{cases} Y'_{12} = Y'_{21} \\ Y'_{11} = Y'_{22} \end{cases}$$

To find Y'$_{11}$ and Y'$_{21}$ y short the output terminals and connect a current source I'$_1$ to the input terminals. The resulting circuit diagram is as shown in Figure 2-32.d

$$Y'_{11} = \left.\frac{I_1'}{V'_1}\right|_{V'_2=0}$$

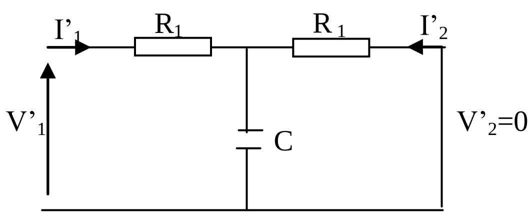


Figure 2-32.d

Applying KVL to the loop, we get

$$V'_1 = Z_{R1}I'_1 + (Z_{R1} // Z_C)I'_1$$

$$\Rightarrow \frac{I'_1}{V'_1} = \frac{1}{Z_{R1} + (Z_{R1} // Z_C)}$$

$$Z_{R1} // Z_C = \frac{R_1 \times \frac{1}{JC\omega}}{R_1 + \frac{1}{JC\omega}} = \frac{R_1}{1 + JR_1C\omega}$$

$$\Rightarrow \frac{I'_1}{V'_1} = \frac{1}{R_1 + \frac{R_1}{1 + JR_1C\omega}} = \frac{1 + JR_1C\omega}{(1 + JR_1C\omega)R_1 + R_1}$$

$$Y'_{11} = \frac{1 + JR_1C\omega}{R_1(2 + JR_1C\omega)} = Y'_{22}$$

$$Y'_{12} = \left.\frac{I'_1}{V'_2}\right|_{V_2'=0} = ?$$

Applying KVL to the loop, we get

$$V'_1 - Z_{R1}I'_1 + Z_{R1}I_2' = 0$$
$$V'_1 = Z_{R1}I'_1 - Z_{R1}I_2'$$

Using the principle of current division $I_2' = -\frac{Z_C}{Z_C + Z_{R1}} I_1' \Rightarrow I_1' = -\frac{Z_C + Z_{R1}}{Z_C} I_2'$

$$V'_1 = -\frac{Z_{R1}}{Z_C}\left(Z_C + Z_{R1}\right)I_1' - Z_{R1}I_1'$$

$$\frac{I_1'}{V'_1} = -\frac{1}{\frac{Z_{R1}}{Z_C}\left(Z_C + Z_{R1}\right) + Z_{R1}}$$

$$\frac{I_1'}{V'_1} = -\frac{1}{\frac{R_1}{\frac{1}{JC\omega}}\left(\frac{1}{JC\omega} + R_1\right) + R_1} = -\frac{1}{R_1 JC\omega\left(\frac{1 + R_1 JC\omega}{JC\omega}\right) + R_1}$$

$$= -\frac{1}{R_1\left(1 + R_1 JC\omega\right) + R_1}$$

$$Y_{12}' = -\frac{1}{JR_1^{\,2}C\omega + 2R_1} = Y_{21}$$

$$Y' = \begin{bmatrix} \frac{1 + JR_1C\omega}{R_1\left(2 + JR_1C\omega\right)} & \frac{1}{JR_1^{\,2}C\omega + 2R_1} \\ \frac{1}{JR_1^{\,2}C\omega + 2R_1} & \frac{1 + JR_1C\omega}{R_1\left(2 + JR_1C\omega\right)} \end{bmatrix}$$

Two-Port Bridged

For this two-port network, which is passive and symmetric **Figure 2-32.c**

, we can write:

$$\begin{cases} I''_1 = Y''_{11}V''_1 + Y''_{12}V''_2 \\ I''_2 = Y''_{21}V''_1 + Y''_{22}V''_2 \end{cases} \qquad (B) \qquad \begin{cases} Y''_{12} = Y''_{21} \\ Y''_{11} = Y''_{22} \end{cases}$$

Applying KVL to the loop, we get (Figure 2-32.c)

$$\begin{cases} I''_1 = -I''_2 \\ V''_1 - V''_2 = R_2 I''_1 \end{cases} \quad ou \quad \begin{cases} I''_1 = \frac{1}{R_2}V''_1 - \frac{1}{R_2}V''_2 \\ I''_2 = -\frac{1}{R_2}V''_1 + \frac{1}{R_2}V''_2 \end{cases} \qquad (C)$$

Comparing equations B and C with

$$(Y'') == \begin{pmatrix} \frac{1}{R_2} & -\frac{1}{R_2} \\ -\frac{1}{R_2} & \frac{1}{R_2} \end{pmatrix}$$

$$[Y] = \begin{bmatrix} Y''_{11} + Y'_{11} & Y''_{12} + Y'_{12} \\ Y''_{21} + Y'_{21} & Y''_{22} + Y'_{22} \end{bmatrix} = \begin{bmatrix} \frac{1 + JR_1C\omega}{R_1(2 + JR_1C\omega)} + \frac{1}{R_2} & \frac{1}{JR_1^{\,2}C\omega + 2R_1} - \frac{1}{R_2} \\ \frac{1}{JR_1^{\,2}C\omega + 2R_1} - \frac{1}{R_2} & \frac{1 + JR_1C\omega}{R_1(2 + JR_1C\omega)} + \frac{1}{R_2} \end{bmatrix}$$

Exercise 2.5: Determination of a Transfer Matrix by Cascade Decomposition

1- Calculate the transmission parameters of figure using the short-circuit and open-circuit method.

Using the equation for T-parameters for a-network

To determine **A** and **C**, we leave the output port open as in Figure 2-34.a so that $I_2 = 0$ and place a voltage source at the input port. We have

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0}$$

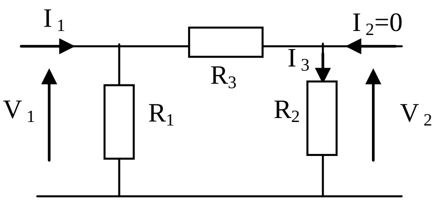


Figure 2-3.a

Using the principle of voltage division,

$$V_2 = \frac{R_3}{R_2 + R_3}V_1 \qquad R_1 = R_2 = R_3 = R$$

$$V_2 = \frac{R}{2R}V_1 = \frac{1}{2}V_1$$

$$A = \left(\frac{V_1}{V_2}\right)_{I_1=0} = \frac{V_1}{\frac{1}{2}V_1} = 2$$

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = ?$$

Applying KVL to the right-mesh, we get

$$V_2 = R_2 I_3 = RI_3$$

Using the principle of Current division,

$$I_3 = \frac{R_1}{R_1 + R_2 + R_3} I_1 \qquad R_1 = R_2 = R_3 = R$$

$$I_3 = \frac{R}{3R} I_1 = \frac{1}{3} I_1$$

$$V_2 = R\frac{1}{3} I_1$$

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = \frac{I_1}{\frac{R}{3} I_1} = \frac{3}{R}$$

To find the parameters **B** and **D**, short-circuit the output port and connect a voltage source V_1 to the input port as shown in figure 2-33.b.

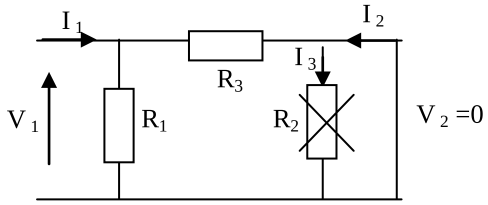


Figure 2-33.b

$$B = -\left.\frac{V_1}{I_2}\right|_{V_2=0} = ?$$

Applying KVL to the right-mesh, we get

$$V_1 = (R_1 // R_3) I = \frac{R^2}{2R} I_1 = \frac{R}{2} I_1 \qquad R_1 = R_2 = R_3 = R$$

Using the principle of Current division,

$$I_2 = -\frac{R_1}{R_1 + R_3} I_1 = -\frac{R}{2R} I_1 = -\frac{1}{2} I_1 \Rightarrow I_1 = -2I_2$$

$$V_1 = (R_1 // R_3) I_1 = \frac{R^2}{2R} I_1 = -\frac{2R}{2} I_2 = -RI_2$$

$$B = \left.\frac{V_1}{I_2}\right|_{V_2=0} = \frac{RI_2}{I_2} = R$$

$$D = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = ? \qquad D = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = \frac{2I_2}{I_2} = 2$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 2 & R(\Omega) \\ \frac{3}{R}(S) & 2 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

1- Cascade association of two two-port networks

To determine **A**' and **C**', we leave the output port open as in Figure 2-33.c so that $I_2 = 0$ and place a voltage source at the input port. We have

$$A' = \left.\frac{V_1}{V_2}\right|_{I_2=0} = ?$$

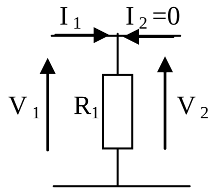


Figure 2-33.c

Applying KVL to the right-mesh, we get

$$V_1 = R_1 I_1 = RI_1 = V_2$$

$$A' = \left.\frac{V_1}{V_2}\right|_{I_2=0} = \frac{V_1}{V_1} = 1$$

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = ?$$

Applying KVL to the right-mesh, we get

$$V_2 = R_1 I_1 = RI_1$$

$$C' = \left.\frac{I_1}{V_2}\right|_{I_2=0} = \frac{I_1}{RI_1} = \frac{1}{R}$$

To find the parameters **B**' and **D**', short-circuit the output port and connect a voltage source V_1 to the input port as shown in figure 2-33.d.

$$B' = -\left.\frac{V_1}{I_2}\right|_{V_2=0} = ?$$

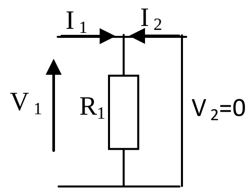


Figure 2-33.d

Applying KVL to the right-mesh, we get

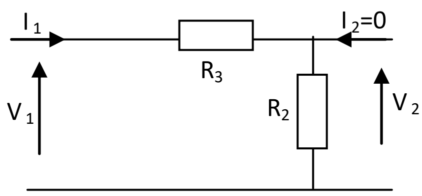
$$V_2 = 0 = V_1$$

$$B'' = -\left.\frac{V_1}{I_2}\right|_{V_2=0} = 0$$

$$D = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = ? \qquad I_1 = -I_2 \qquad D' = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = \frac{I_2}{I_2} = 1$$

$$T_A = \begin{bmatrix} 1 & 0 \\ \frac{1}{R}(S) & 1 \end{bmatrix}$$

To determine **A**" and **C''**, we leave the output port open as in Figure 2-33.e so that $I_2 = 0$ and place a voltage source at the input port. We have



$$A'' = \left.\frac{V_1}{V_2}\right|_{I_2=0} = ?$$

Using the principle of voltage division,

$$V_2 = \frac{R_2}{R_2 + R_3} V_1 = \frac{R}{2R} V_1 = \frac{1}{2} V_1$$

$$A'' = \left.\frac{V_1}{V_2}\right|_{I_2=0} = \frac{V_1}{\frac{1}{2}V_1} = 2$$

$$C'' = \left.\frac{I_1}{V_2}\right|_{I_2=0} = ?$$

Applying KVL to the right-mesh, we get

$$V_2 = R_2 I_1 = R I_1$$

$$C'' = \left.\frac{I_1}{V_2}\right|_{I_2=0} = \frac{I_1}{R I_1} = \frac{1}{R}$$

To find the parameters **B**" and **D**", short-circuit the output port and connect a voltage source V_1 to the input port as shown in figure 2-33.f.

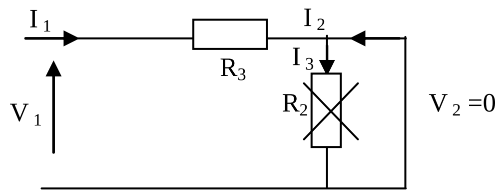


Figure 2-33.f

$$B = -\left.\frac{V_1}{I_2}\right|_{V_2=0} = ?$$

Applying KVL to the right-mesh, we get

$$V_1 = -R_3 I_2 = -R I_2$$

$$B'' = \left.\frac{V_1}{I_2}\right|_{V_2=0} = \frac{R I_2}{I_2} = R$$

$$D'' = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = ? \qquad I_1 = -I_2 \qquad D''' = -\left.\frac{I_1}{I_2}\right|_{V_2=0} = \frac{I_2}{I_2} = 1$$

For B $$T_B = \begin{bmatrix} 2 & R(\Omega) \\ \frac{1}{R}(S) & 1 \end{bmatrix}$$

Overall T

$$T = T_A \times T_B = \begin{pmatrix} A^{'} & C^{'} \\ C^{''} & D^{'} \end{pmatrix} \times \begin{pmatrix} A^{''} & B^{''} \\ C^{'''} & D^{''} \end{pmatrix} = \begin{pmatrix} A^{'}A^{''} + B^{'}C^{''} & A^{'}B^{''} + B^{'}D^{''} \\ C^{'}A^{''} + D^{'}C^{''} & C^{'}B^{''} + D^{'}D^{''} \end{pmatrix}$$

$$T = T_A \times T_B = \begin{pmatrix} 1 & 0 \\ \frac{1}{R} & 1^{'} \end{pmatrix} \times \begin{pmatrix} 2 & R \\ \frac{1}{R} & 1 \end{pmatrix} = \begin{pmatrix} 1\times 2 + 0\times\frac{1}{R} & 1\times R + 0\times 1 \\ \frac{1}{R}\times 2 + 1\times\frac{1}{R} & \frac{1}{R}\times R +^{'} 1\times 1 \end{pmatrix} = \begin{pmatrix} 2 & R \\ \frac{3}{R} & 2 \end{pmatrix}$$

Exercise 2. Low-Pass Filtre

a- transfer function of the circuit in Figure 2-34 and express it in the

To By applying the voltage divider Rule, we can determine. The transfer function

$$V_o = \frac{Z_C}{Z_R + 2Z_C} V_I = \frac{\frac{1}{jC\omega}}{R + \frac{2}{jC\omega}} V_I$$

$$\frac{V_O}{V_I} = \frac{\frac{1}{jC\omega}}{\frac{jRC\omega + 2}{jC\omega}} = \frac{1}{jRC\omega + 2} = \frac{1}{2}\frac{1}{j\frac{RC\omega}{2} + 1}$$

$$\frac{V_O}{V_I} = A\frac{1}{j\frac{\omega}{\omega_0} + 1} \qquad (A) \qquad A = \frac{1}{2} \qquad \omega_0 = \frac{2}{RC}$$

The Bode plot

From Eq. (A), The magnitude of the transfer function (Gain) is:

$$|H(j\omega)| = \left|\frac{1}{2}\frac{1}{j\frac{\omega}{\omega_0} + 1}\right| = \frac{1}{2}\frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}}$$

$$G(\omega)_{dB} = 20\log|H(j\omega)| = 20\log\frac{1}{2}\frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}} = 20\log\frac{1}{2} + 20\log\frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}}$$

$$G(\omega)_{dB} = 20\log 1 - 20\log 2 + 20\log 1 - 20\log\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}$$

$$G(\omega)_{dB} = -20\log - 20\log\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} = -6dB - 20\log\left(1 + \left(\frac{\omega}{\omega_0}\right)^2\right)^{\frac{1}{2}}$$

$$G(\omega)_{dB} = -6dB - \frac{1}{2} \times 20\log\left(1+\left(\frac{\omega}{\omega_0}\right)^2\right) = -6dB - 10\log\left(1+\left(\frac{\omega}{\omega_0}\right)^2\right)$$

Phase Plot

The argument of the transfer function (Phase) is:

$$\varphi(\omega) = \arg[H(\omega)] = \arg\left[\frac{\frac{1}{2}}{1 - j\frac{\omega_0}{\omega}}\right] = \arg\left[\frac{1}{2}\right] - \arg\left[1 - j\frac{\omega}{\omega_0}\right]$$

$$\varphi(\omega) = arctg[0] + arctg\left[\frac{\omega}{\omega_0}\right] = arctg\left[\frac{\omega}{\omega_0}\right]$$

ω	**0**	$\frac{\omega}{\omega_C}$	ω_C	$10\omega_C$	∞
$\lvert H(j\omega)\rvert$	1	-	$\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{10}}$	0
$\lvert G_1(j\omega)\rvert_{dB} = 20\log\lvert H(j\omega)\rvert$	0	-	-3dB	-20dB	$-\infty$
$\lvert G_1(j\omega)\rvert_{dB} = -6dB + 20\log\lvert H(j\omega)\rvert$	-6dB	-	-9dB	-26dB	$-\infty$
φ	0	-	$-\frac{\pi}{4}$	-	$-\frac{\pi}{2}$

Figure 2-36 shown the Bode plots for magnitude plot and phase plot

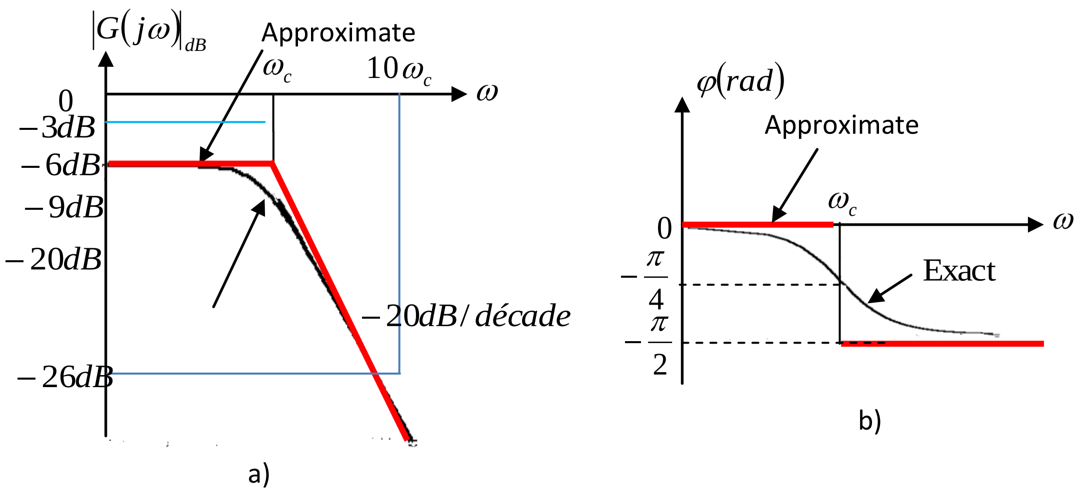


Figure 2.36 *:* Bode plots : (a) magnitude plot, (b) phase plot

Chapter 03

DIODE

3 DIODE

Learning Objectives

By studying this chapter and completing the related exercises, you will be able to:

1. Understand the introduction and basic concepts of semiconductors.
2. Define a diode and understand its function in electronic circuits.
3. Recognize and draw the symbol of a diode.
4. Understand the concepts of forward bias and reverse bias in diode operation.
5. Understand the process of semiconductor doping.
6. Explain the formation and operation of the PN junction.
7. Analyze the operating principle of a diode.
8. Study the current- voltage characteristics of a diode.
9. Understand diode biasing methods and their effects on circuit behavior.
10. Explore various applications of diodes in electronic circuits.
11. Understand the analysis methods and wide range of applications of Zener diodes.
12. Identify and differentiate between the different types of diodes

3.1 The atom

An atom is the smallest unit of matter that preserves the properties of an element. Its nucleus contains positively charged protons and neutral neutrons, while negatively charged electrons move around the nucleus in specific energy levels or shells, as shown in Figure 3-1

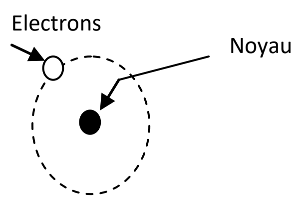


Figure 3-1: Structure atomique (Modèle de Bohr)

- Electrons with the highest energy levels exists in the outermost shell of an atom and are loosely bound to the atoms:
- This outermost shell is known as the valence shell and electrons in the shell are called valence electrons
- When an electron gains a certain amount of energy, it moves to an orbit farther from to nucleus
- The process of losing an electron is called ionization
- The escaped valence electron is called a free electron

3.2 Insulators, Conductors, and Semiconductors

Materials can be divided into three categories according to their ability to conduct an electric current:

- **Insulators**

An insulator is a material that does not conduct electrical current under normal conditions. Most effective insulators are compounds with very high resistivity, and their valence electrons are firmly bound to their atoms. Common examples include rubber, plastics, glass, mica, and quartz (Figure 3-2.a).

- **Conductors**

A conductor is a material that **readily** allows electrical current to flow. Most metals are good conductors, with the best being **single-element** materials such as copper (Cu), silver (Ag), gold (Au), and aluminum (Al). These materials have atoms with a single valence electron that is very **loosely** bound, making it easy for electrons to move (Figure 3-2.c).

- **Semiconductors**

A **semiconductor** is a material whose ability to conduct electric current lies between that of a conductor and an insulator. **Single-element** semiconductors consist of atoms with **four valence electrons**, with **silicon** being the most commonly used (Figure 3-2.b).

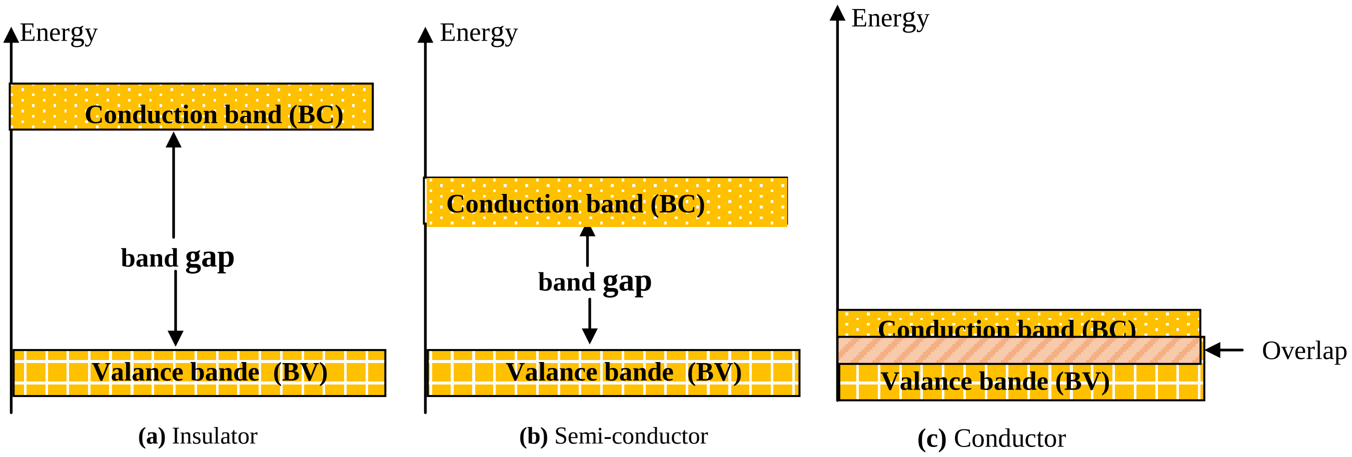


Figure 3-2: Energy diagrams for the three types of materials.

Semiconductors are crystalline materials the are characterized by specific energy bands for electrons. Between the bands are gaps; these gaps represent energies that electrons cannot a have. The last energy band is the conduction band, where electrons mobile. The next to the last band is valence band, which is the energy level associated with electrons involved bonding

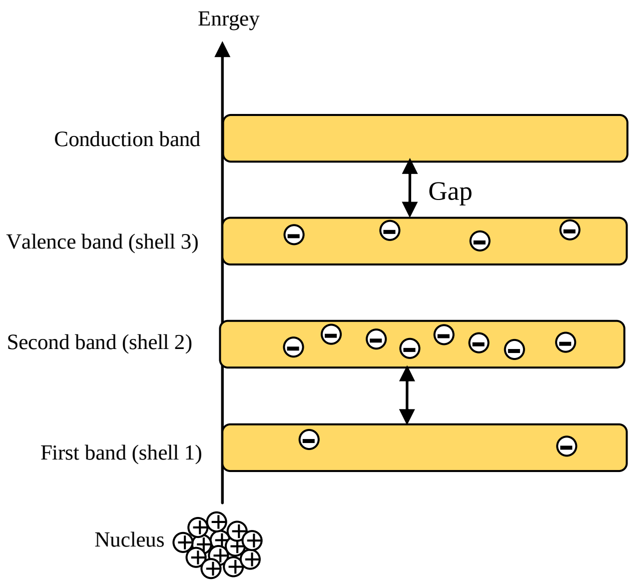
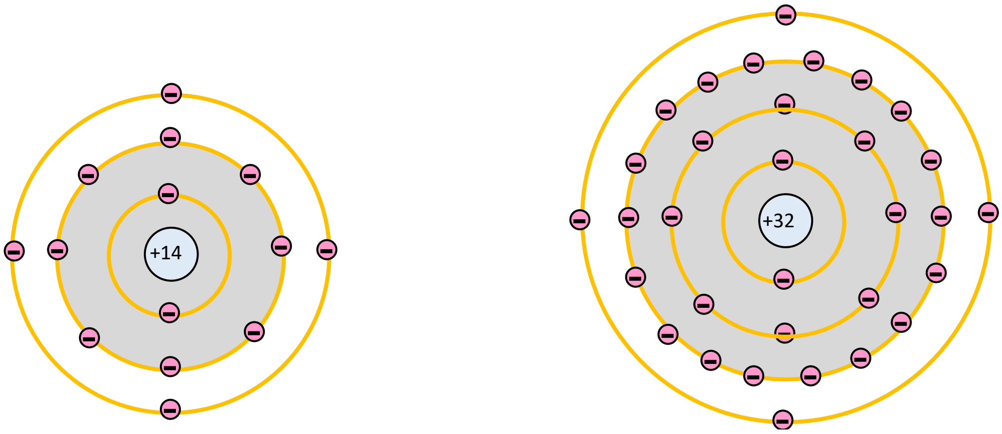


Figure 3-3: Energy band diagram for an unexcited atom in a pure (intrinsic) silicon crystal

3.3 Comparison of a Semiconductor Atom to a Conductor Atom

Both silicon and germanium atoms have four valence electrons. However, they differ in their atomic structure: silicon has 14 protons in its nucleus, while germanium has 32. The valence electrons in germanium occupy the fourth shell, whereas those in silicon are in the third shell and therefore closer to the nucleus. As a result, the valence electrons in germanium are at a higher energy level and are less tightly bound to the nucleus. This means that only a small amount of additional energy is needed to free them. Consequently, germanium becomes more unstable at high temperatures.



Silicon atoms Germanium atoms

Figure 3-4: Diagrams of the silicon and germanium atoms

3.4 Covalent band in a intrinsic silicon crystal

A covalent bond is a type of chemical bond where two atoms share one or more pairs of electrons to achieve stability.

In an intrinsic silicon crystal, each silicon atom is bonded to four neighboring atoms through covalent bonds, where each atom shares its four valence electrons with its neighbors to form a stable crystal structure**.**

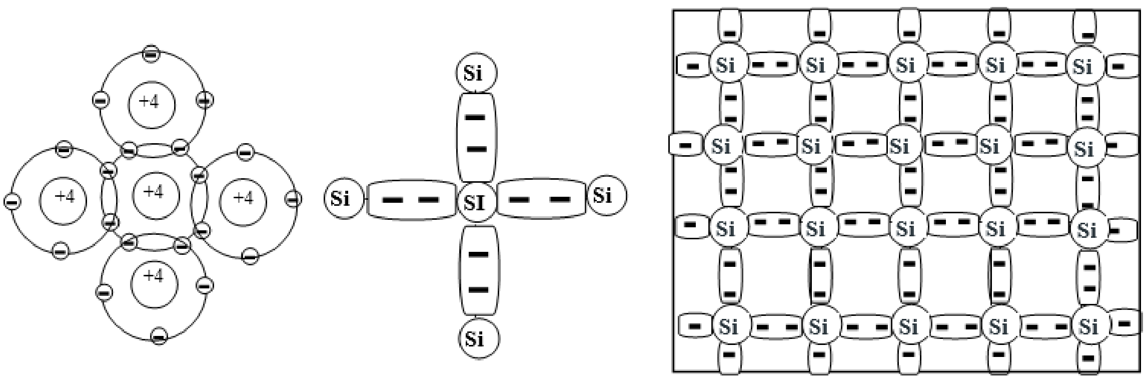


Figure 3-5 : Covalent bonds in a silicon crystal

Note:

Covalent bonding in germanium is similar because it also has four valence electrons.

3.5 Types of semicoductors

Semiconductors can be classified into **two types** on the basis of purity (Figure 3-6).

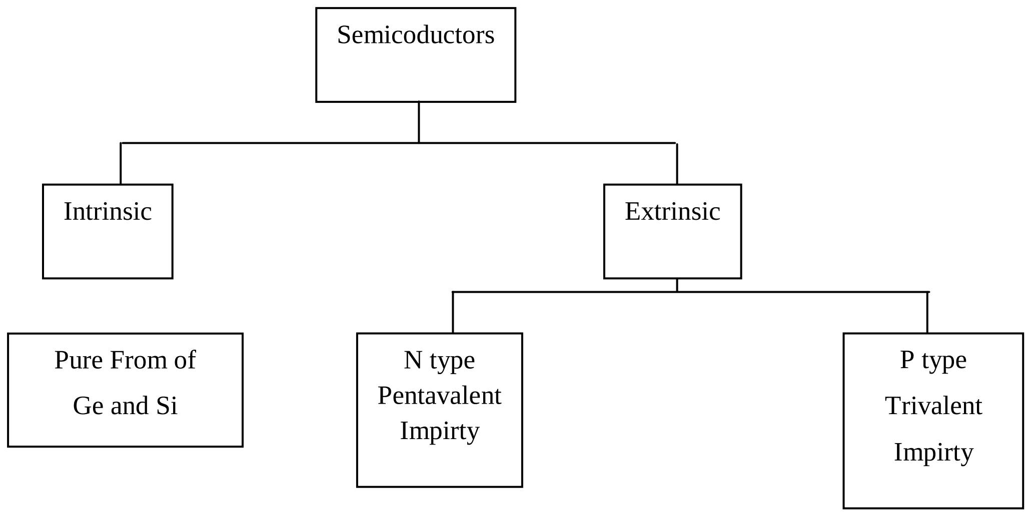


Figure 3-6 : : Types of semicoductors

- **Current in semiconductors**

Figure 3-8 shows the energy band diagram for an unexcited atom (no external energy such as heat) in a pure silicon crystal. This condition exists only at absolute zero temperature (0 Kelvin).

At this temperature:

All electrons remain in the valence band.

The conduction band is completely empty because no electrons have enough energy to move up to it.

Therefore, no electrical conduction occurs the crystal behaves as a perfect insulator.

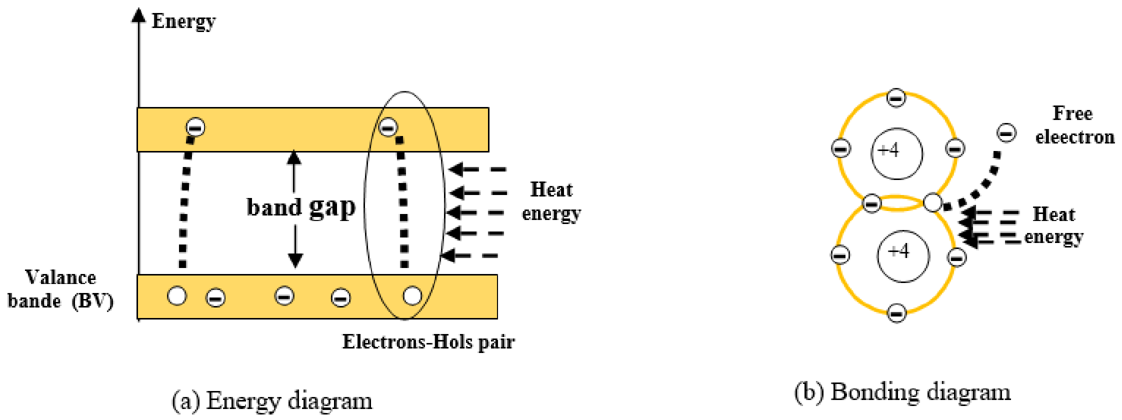


Figure 3-7: Creation of electron-hole pairs in a silicon crystal

In an intrinsic (pure) silicon crystal at room temperature, the thermal energy is sufficient for some valence electrons to jump across the energy gap from the valence band to the conduction band, where they become free electrons. These free electrons are also known as conduction electrons

When an electron jumps to the conduction band, a vacancy is left in the valence band within the crystal. This vacancy is known as a hole. Each time an electron is lifted to the conduction band by external energy, it leaves behind one hole in the valence band, forming what is called an electron-hole pair. Recombination takes place when an electron in the conduction band loses energy and drops back into a hole in the valence band.

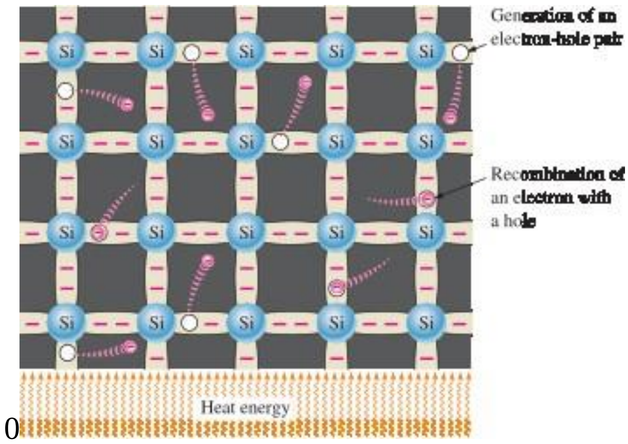


Figure 3-8 : Electron-hole pairs in a silicon crystal

When a voltage is applied across intrinsic silicon (Figure 3-9**)**, the free electrons in the conduction band and the holes in the valence band move under the influence of the electric field, generating an electric current. Electrons, being negatively charged, move toward the positive terminal, while holes, behaving like positive charges, move toward the negative terminal.

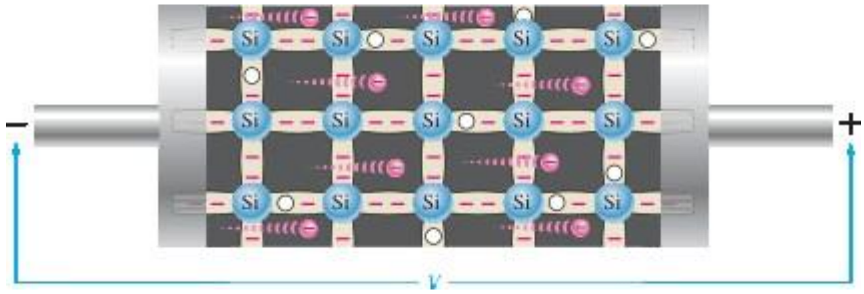


Figure 3-9 : Electron and Hole Current

a-Electron Current

Electrons in the conduction band are free to move.

When an electric field is applied, these free electrons drift toward the positive terminal. Their movement forms the electron current, which is a major part of the total current.

In short:

Electron current = flow of free electrons in the conduction band.

b.Hole Current

A hole is the absence of an electron in the valence band.

When an electron moves to fill a hole, the hole appears to move in the opposite direction of the electron. Under applied voltage, holes drift toward the negative terminal. This movement forms the hole current.

In short:

Hole current = movement of holes in the valence band (opposite to electron motion).

3.6 P-Type Semiconductor and N-Type Semiconductor

Doping is the process of adding a small amount of impurity atoms to a pure (intrinsic) semiconductor to increase its electrical conductivity. Introducing these impurities into intrinsic silicon boosts the number of charge carriers, creating either more electrons or more holes within the crystal.

There are two main types of extrinsic semiconductors, depending on the type of dopant used:

- N-type Semiconductors
- P-type Semiconductors

3.6.1 N-type Semiconductors:

To increase the number of conduction-band electrons in intrinsic silicon, pentavalent impurities are added, forming an n-type semiconductor. These impurities have five valence electrons and include atoms such as arsenic (As), phosphorus (P), bismuth (Bi), and antimony (Sb). The dopant atom integrates into the semiconductor crystal; however, to form bonds with neighboring atoms, only 4 electrons are needed. The fifth electron is therefore in excess and has no bonding role. This is why the dopant is called a **donor (N-type)** of electrons (negative charge carriers). It should be noted that when this extra electron leaves its atom, it leaves behind a **fixed positive ion (**Figure 3-10)

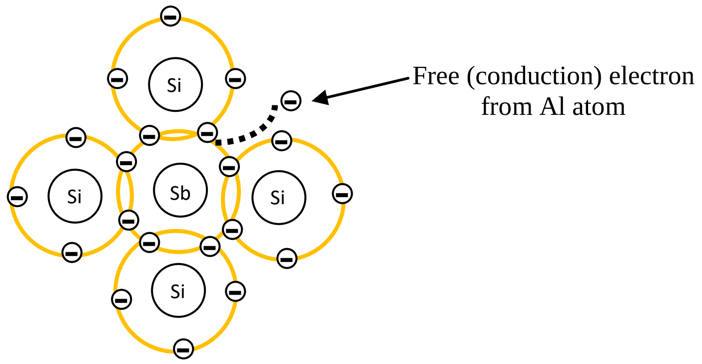


Figure 3-10 : Antimony impurity in n-type

3.6.2 P-type Semiconductors

To increase the number of holes in intrinsic silicon, trivalent impurity atoms are added, creating a p-type semiconductor. These impurities have three valence electrons and include elements such as boron (B), indium (In), and gallium (Ga).The dopant atom integrates into the semiconductor crystal; however, to form bonds with neighboring atoms, 4 electrons are required, while the dopant only has 3. Therefore, a vacant spot (hole) available can accept an electron. An electron from a neighboring atom can fill this hole. The dopant atom then becomes a fixed negative ion, and the atom that lost the electron ends up with a hole and a positive excess charge. This is why the dopant is called an **acceptor** (P-type) of electrons (Figure 3-11).

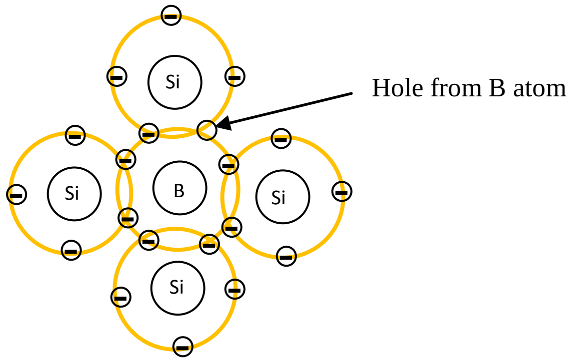


Figure 3-11 : Antimony impurity in P-type material

3.7 P-N Junction

The PN junction is the fundamental element of electronic components (diodes, transistors, thyristors, etc.). The PN junction is the region that separates two extrinsic semiconductors of different types: P-type (rich in holes) and an N-type (rich in electrons) (Figure 3-12)

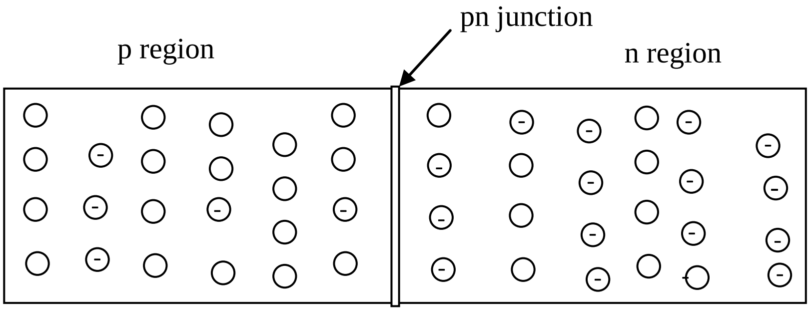


Figure 3-12 : The pn junction

3.8 Non-polarized P-N junction

Before the pn junction is formed, the n-type material contains equal numbers of electrons and protons, so it has no net electric charge. The same condition applies to the p-type material, which is also electrically neutral **.** After the pn junction is formed, the n-type region loses free electrons as they diffuse across the junction into the p-type region. This process results in the formation of a layer of positive charges (pentavalent ions) near the junction. As electrons cross the junction, the p-type region loses holes due to the recombination of electrons and holes. This results in the formation of a layer of negative charges (trivalent ions) near the junction. Together, these layers of positive and negative charges create the depletion region. Eventually, equilibrium is reached, and electron diffusion across the junction ceases

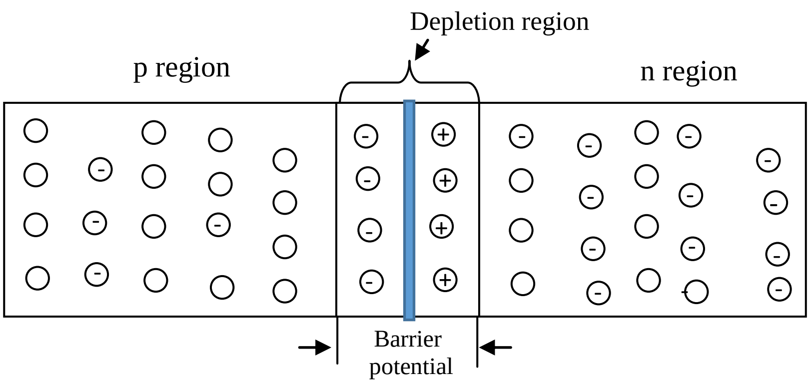


Figure 3-13 : Non-polarized P-N junction at equilibrium

An electric field across the depletion region. This electric field acts as a barrier for the free electrons in the n-type region, requiring energy to push an electron through it. At 25°C, the typical barrier potential is about 0.7 V for silicon and 0.3 V for germanium.

3.9 What Is a Diode?

A diode consists of a small piece of semiconductor, typically silicon, with one half doped as a p-type region and the other half as an n-type region, forming a pn junction with a depletion region in between. The p region is called the anode and is connected to a conductive terminal. The n region is called the cathode and is connected to a second conductive terminal. The fundamental structure and schematic symbol of a diode are illustrated in Figure 3-14.

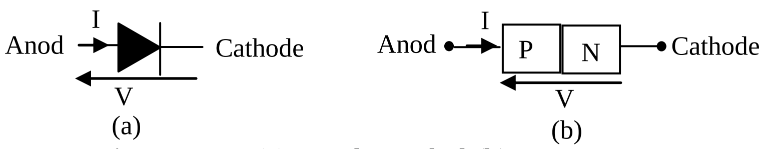


Figure 3-14: (a) Diode symbol (b) PN junction.

3.10 Diode operation

3.10.1 Forword Bias

Forward bias is the condition in which a pn junction allows current to flow, with the negative terminal of V_{BIAS} connected to the n region of the diode and the positive terminal connected to the p region (Figure 3-15).

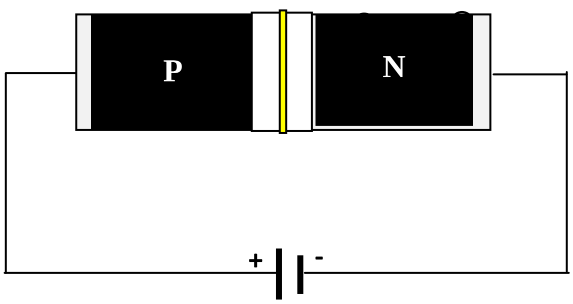


Figure 3-15 : A diode connected for forward bias

The applied bias voltage provides enough energy for the free electrons to overcome the depletion-region barrier and enter the p region. Once there, these conduction electrons lose sufficient energy and immediately recombine with holes in the valence band. Meanwhile, the positive terminal of the bias voltage attracts valence electrons toward the left side of the p region. These electrons move from hole to hole in that direction, and as they exit the p region, they leave behind new holes.

As electrons flow into the depletion region, the number of positive ions decreases. Similarly, as holes move into the depletion region, the number of negative ions decreases.

This reduction of both positive and negative ions under forward bias causes the depletion region to narrow.

3.10.2 Reverse bias

Reverse bias is the condition that effectively prevents current from flowing through the diode. In this configuration, the positive terminal of the applied voltage is connected to the n region of the diode, while the negative terminal is connected to the p region (Figure 3-16).

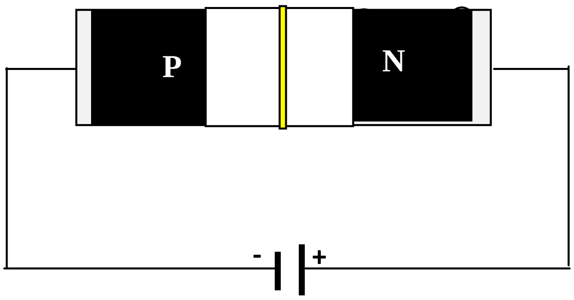


Figure 3-16 : A diode connected for reverse bias

In the n region, electrons are drawn toward the positive terminal of the voltage source, leaving behind additional positive ions. This process widens the depletion region and reduces the concentration of majority carriers. In the p region, electrons supplied by the negative terminal move from hole to hole toward the depletion region, where they create additional negative ions. This also causes the depletion region to widen and further reduces the number of majority carriers. As the depletion regions in both the n and p materials expand, the electric field between the fixed positive and negative ions becomes stronger. Eventually, the potential across the depletion region equals the applied bias voltage V_{BIAS}. At this point, the transition current effectively stops.

3.10.2.1 Reverse current

The very small current that remains under reverse-bias conditions after the transition current has vanished is due to minority carriers in the n and p regions. These carriers originate from thermally generated electron–hole pairs.

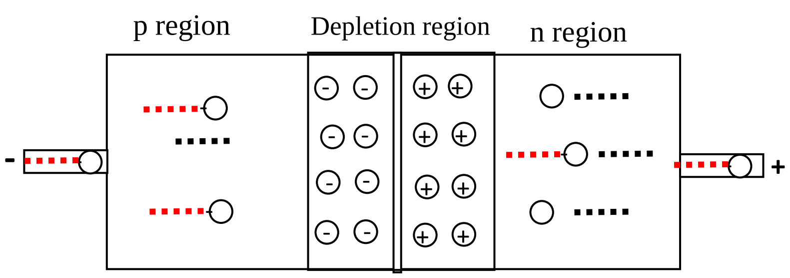


Figure 3-17 : Reverse currennt

3.10.2.2 Reverse Breakdown

If the external reverse-bias voltage is increased to a value called the **breakdown voltage**, the reverse current will drastically increase. The high reverse-bias voltage imparts energy to the free minority electrons so that as they speed through the p region, they collide with atoms with enough energy to knock valence electrons out of orbit and into the conduction band. The newly created conduction electrons are also high in energy and repeat the process. The multiplication of conduction electrons just discussed is known as the **avalanche effect.**

3.11 Voltage current characteristic of diode

3.11.1 I-V Characteristic for Forward Bias

When a diode is biased in the forward direction, current flows through it. This current is known as the **forward current I_F**.

The diode forward voltage V_F is plotted along the horizontal axis, increasing to the right, while the forward current I_F is plotted along the vertical axis, increasing upward. Point **A** represents the zero-bias condition. Point **B** corresponds to a forward voltage that is less than the barrier potential of 0.7 V, where only a very small current flows. Point **C** occurs when the forward voltage is approximately equal to the barrier potential. As the applied forward-bias voltage increases beyond this knee point, the forward current rises rapidly, while the forward voltage increases only slightly above 0.7 V.

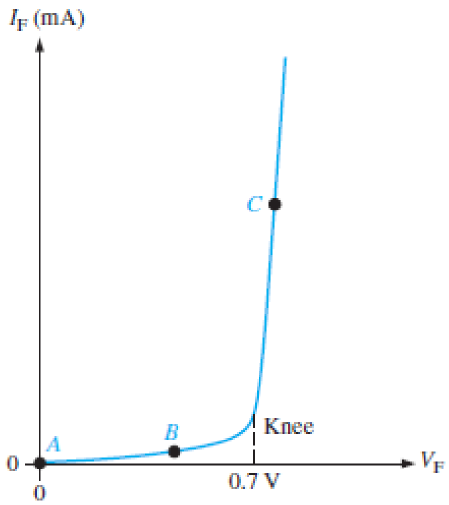


Figure 3-18 : I-*V* characteristic curve for forward bias.

3.11.2 I-V Characteristic for Reverse Bias

When a reverse-bias voltage is applied across a diode, only a very small reverse current I_R flows through the pn junction. At 0 V across the diode, there is no reverse current. As V_R is gradually increased, a tiny reverse current begins to flow, and the voltage across the diode rises. When the applied reverse-bias voltage reaches the breakdown voltage V_{BR}, the reverse current I_R increases rapidly. Beyond this point, as V_R continues to increase, the current continues to rise very quickly, while the voltage across the diode increases only slightly above V_{BR}.

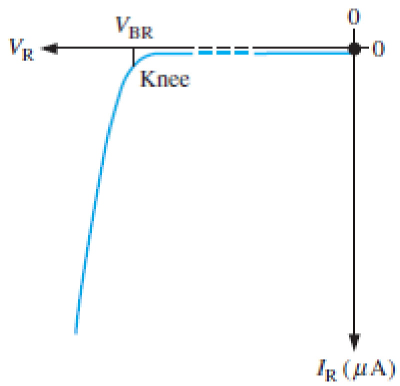


Figure 3-19 : I-*V* characteristic curve for reverse bias

3.12 Diode modeling

3.12.1 Shockley diode model

The Shockley diode equation expresses the relationship between the diode current I_D of a p–n junction and the applied diode voltage V_D, this relationships is the diode I-V characterist

$$I = I_S\left(e^{\frac{qV_D}{nV_T}} - 1\right) \qquad (3.1)$$

I_S The reverse saturation current

I_D: the current through the diode

V_D : Diode terminal. Voltage (V)

k : Boltzman's constante k: $1,38.10^{-23}\ j/°K$:

q : electron charge ; $q = 1,6\times10^{-19}C$

T: absolut temperature of p-n junction.

n = 1 for Ge and 2 si for Si bellow the knee of the curve

n = 1 for above the knee of the curve

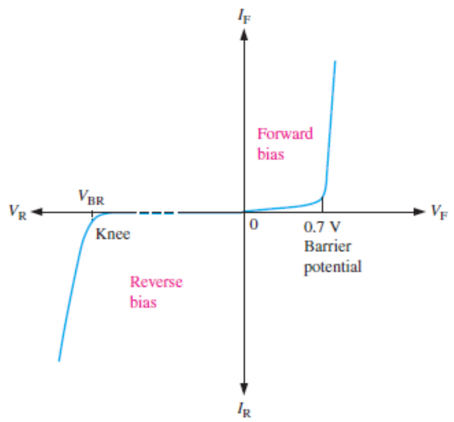


Figure 3-20 : The complete *I-V* characteristic curve for a diode

3.13 Diode equivalent circuit

There are three common levels of approximation used to model a diode in circuit analysis:

- The ideal diode model
- The Practical Diode Model
- The Complete Diode Model

3.13.1 The ideal diode model

The **ideal diode model** is the simplest and least accurate approximation of a diode. In this model, the diode is represented as a **simple switch**: when it is **forward-biased**, it behaves like a **closed (ON) switch**, and when it is **reverse-biased**, it behaves like an **open (OFF) switch**.

.

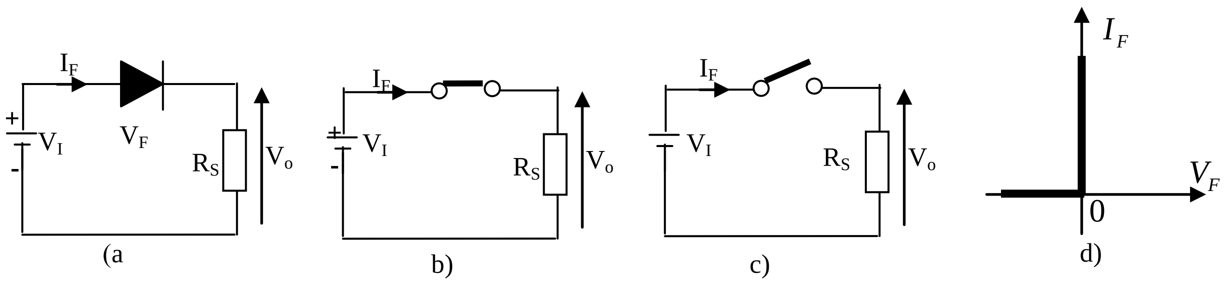


Figure 3-21 : (a) Ideal diode (b) Forward-biased. (c) Reverse –biased and (d) Ideal diode curve

The forward voltage equals the bias voltage

$$V_F = 0 \qquad (3.2)$$

The forward current

$$I_F = \frac{V_{Bias}}{R_L} \qquad (3.3)$$

The reverse current is neglected

$$I_R = 0 \tag{3.4}$$

The reverse voltage equals the bias voltage.

$$V_F = V_{BIAS} \tag{3.5}$$

3.13.2 The Practical Diode Model

The practical diode model takes the barrier potential into account. When the diode is forward-biased, it behaves like a closed switch in series with a small voltage source (V_F) equal to the barrier potential (approximately 0.7 V), with the positive terminal oriented toward the anode, as illustrated in the figure. When the diode is reverse-biased, it behaves like an open switch, the same as in the ideal diode model, as shown in the figure (Figure 3-22)

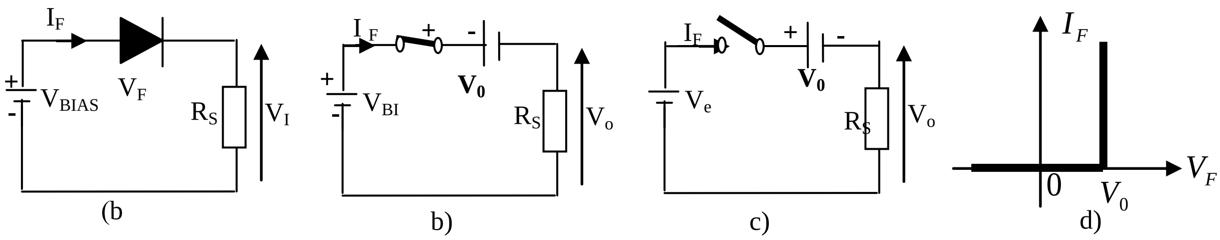


Figure 3-22 : (a) Ideal diode The Practical Diode Model (b) Forward-biased. (c) Reverse-biased. (d) The Practical Diode Model curve

The forward voltage equals the bias voltage

$$V_F = 0{,}7V \tag{3.6}$$

The forward current

$$I_F = \frac{V_{BAIS} - V_F}{R_L} \tag{3.7}$$

The reverse current is neglected

$$I_R = 0 \tag{3.8}$$

The reverse voltage equals the bias voltage.

$$V_F = V_{BIAS} \tag{3.9}$$

3.13.3 The Complete Diode Model

The complete diode model provides the most accurate representation because it includes the barrier potential and the small forward dynamic resistance (r_d'). When the diode is forward-biased, it behaves like a closed switch in series with the equivalent barrier voltage (V_o) and the small forward dynamic resistance. When the diode is reverse-biased, it behaves like an open switch in parallel with a large internal reverse resistance (,r_f').

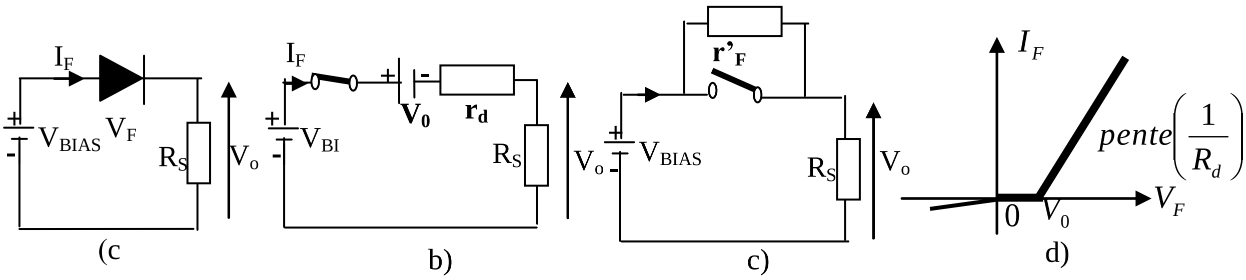


Figure 3-23 : (a) The Practical Diode (b) Forward-biased.
(c) Reverse-biased.(d) The Practical Diode curve

The forward voltage

$$V_F = 0{,}7V \tag{3.10}$$

The forward current

$$I_F = \frac{V_{BAIS} - V_F}{R_L} \tag{3.11}$$

The reverse current is neglected

$$I_R = 0 \tag{3.12}$$

The reverse voltage equals the bias voltage.

$$V_F = V_{BIAS} \tag{3.13}$$

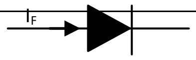
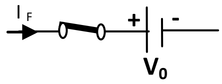
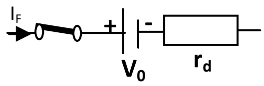
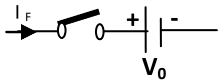
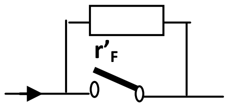
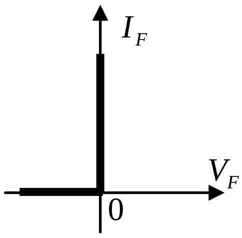
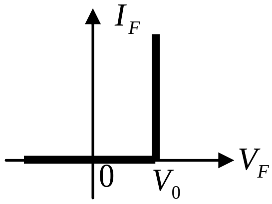
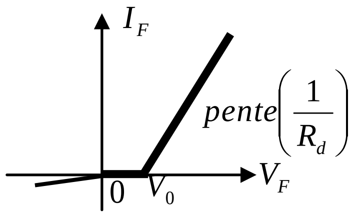
The Dynamic Resistance :

$$r_d = \frac{\Delta V_F}{\Delta I_F} \tag{3.14}$$

3.14 Summary Table

Summary Table 3-1 illustrates the differences between the three diode approximations.

Table 3-1 : Diode Equivalent Circuits (Models)

	The ideal diode model	The Practical Diode model	The complet diode model
Forward bias			
Reverse bias			
Diode curve			

3.15 Load Line

The **load line** is a straight line drawn on the **I-V characteristics curve** of a diode.

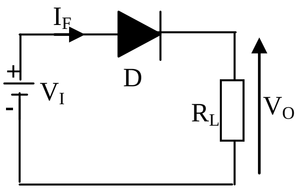


Figure 3-24 : DC Analysis Circuit

Applying KVL

$$E = V_D + R_L I_D \qquad (3.15)$$

This equation is a straight line the **load line**.

$$I_D = \frac{E - V_D}{R_L} \qquad (3.16)$$

When $I_D = 0 \quad \Rightarrow E = V_D \qquad (3.17)$

When $V_D = 0 \quad \Rightarrow I_D = \frac{E}{R_L} \qquad (3.18)$

Theys are two point

Point 1 : $\left(0V, I_D = \dfrac{E}{R_L}\right)$: This point is called saturation because it represents maximum current.

Point 2 : $(E = V_D,\ I_D = 0)$: This point is called cutoff because it represents minimum current.

3.16 The Q-Point

- The point where the **load line** intersects the **diode I–V curve** is called the **operating point** or **Q-point** (Quiescent point).

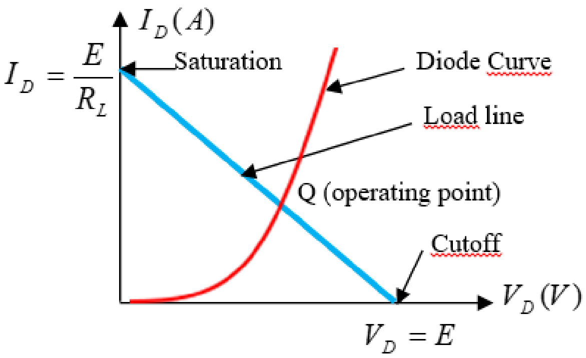


Figure 3-25 : Point is the intersection of the diode curve and the load line

3.17 Diode Applications

Most electronic circuits require a direct voltage to operate. Since the mains supply provides an alternating voltage (**AC**), it is converted into a direct voltage (**DC**) by a circuit called a **power supply** (Figure 3-26).

The different electronic functions for obtaining a continuous signal are:

- ✓ Transformation or adaptation
- ✓ Rectification
- ✓ Filtering
- ✓ Stabilization

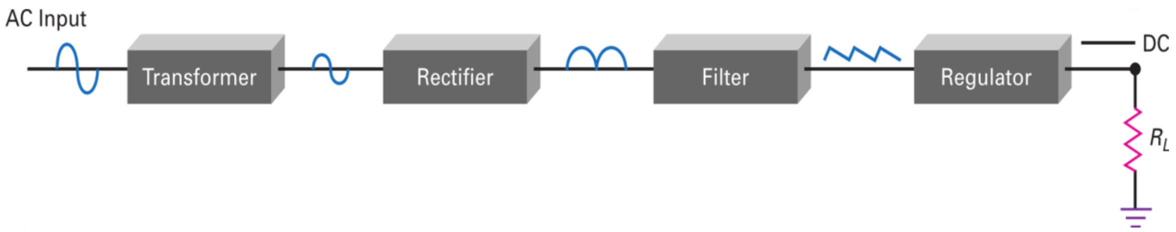


Figure 3-26 : Block diagram showing parts of a power supply

3.17.1 Rectifier Diode

Rectifiers in electronics is the process of converting an (AC) to the (DC),

3.17.1.1 Types of Rectifier

Figure 3-27 illustrates the process of types the rectifier

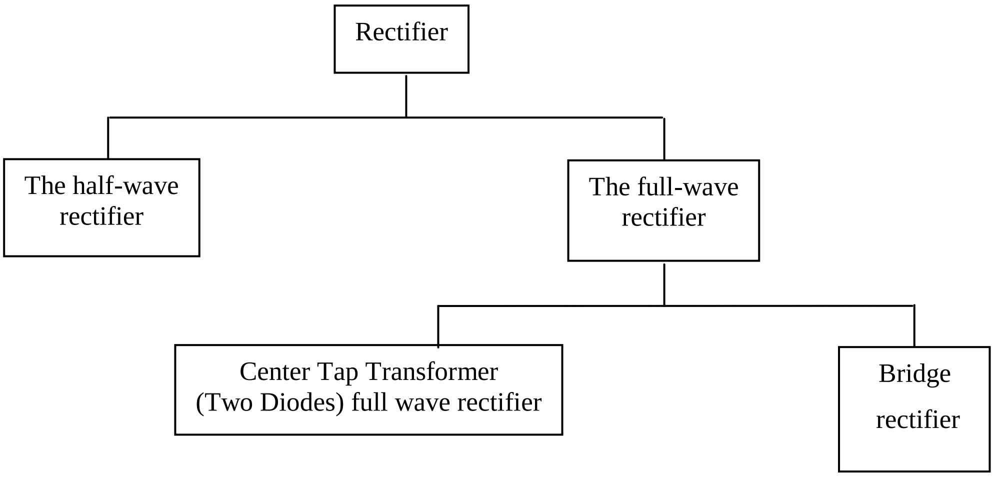


Figure 3-27 : Type of rectifier

- ✓ **The half-wave rectifier**

Figure 3-29 shows the principle of **half-wave rectification**. In this circuit, a diode is connected to an AC source and a load resistor (**R_L**), thereby forming a half-wave rectifier.

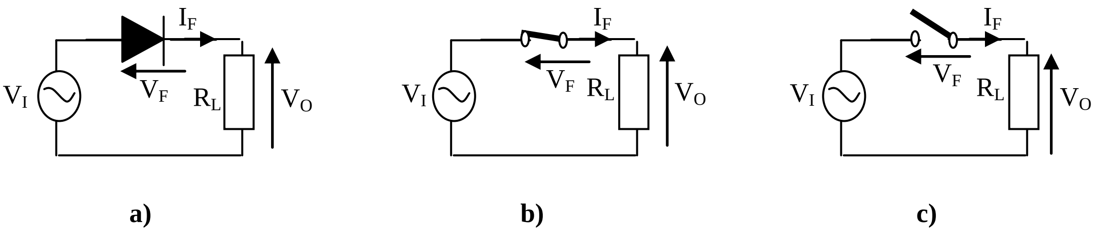


Figure 3-28: a) Ideal half-wave rectifi er; b) on positive half-cycle; c) on negative half-cycle.

- ✓ **Operating principle**

Assumption: We assume that the diode is ideal (V_0=r_d=0)

During the positive hale-cycle: the diode D is forward biased and therefor conducts behaving like a closed switch $\left(i \succ 0 \ et \ V_D = 0\right)$. Hence $\left(V_o = V_I - V_D = V_I\right)$.

During the negative hale-cycle: the diode D is reverse biased and therefore blocked, acting like an open switch. Thus, no current flows. $\left(i = 0 \ et \ V_D = 0\right)$ Hence $\left(V_o = V_I - V_D = 0\right)$

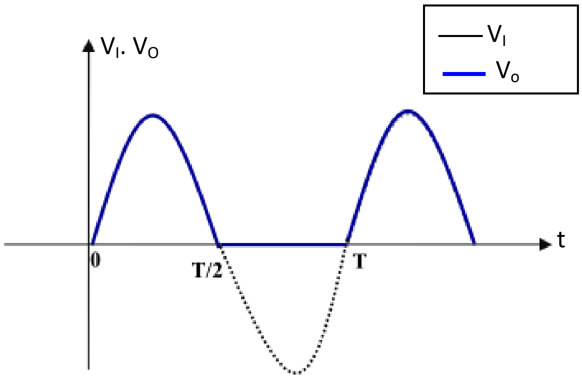


Figure 3-29 : Output Waveform of a Half-Wave Rectifier

3.17.1.2 Full-Wave Rectifier

A full-wave rectifier permits unidirectional current to flow through the load over the entire **360° input cycle**, unlike a half-wave rectifier, which allows current only during **one half of the cycle**. As a result, full-wave rectification produces an output voltage that pulsates every half-cycle and has a frequency **twice that of the input**, as illustrated in Figure 3-30.

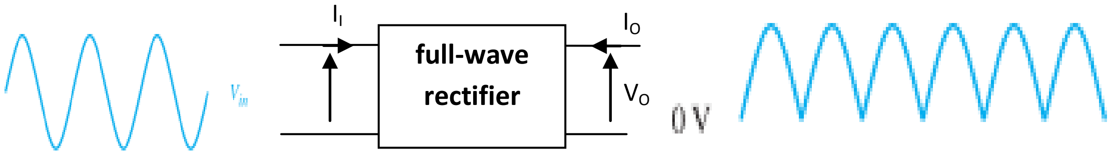


Figure 3-30 : Full-wave rectifier

A-Center-Tapped Full-Wave Rectifier Operation:

A **center-tapped rectifier** is a form of **full-wave rectifier** that employs **two diodes** connected to the secondary winding of a **center-tapped transformer**, as illustrated in Figure 3-31.

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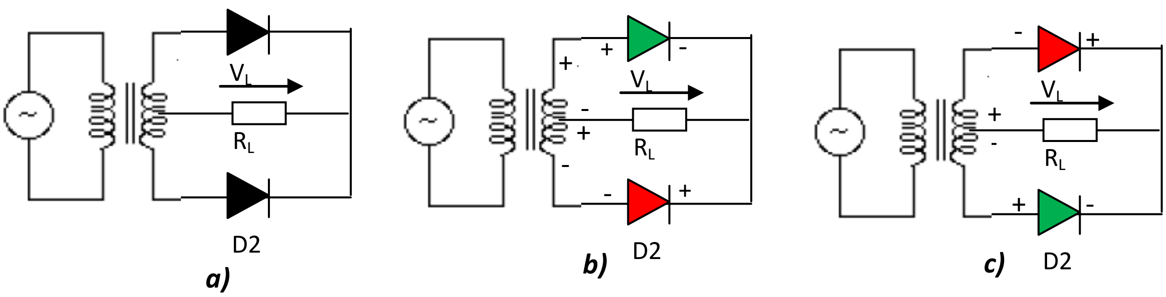


Figure 3-31 : a) A center-tapped full-wave rectifier.b) equivalent circuit for positive half-cycle; c) equivalent circuit for negative half-cycle

Operating principle

Assumption: We assume that the diode is ideal ($V_0=r_d=0$)

- **During the positive hale-cycle:**

Diode D1 is forward-biased $V_o = V_1 = \frac{V_I}{2}$ and Diode D2 is reverse-biased

- **During the positive hale-cycle:**

Diode D1 is is reverse-biased and Diode D2 is forward-biased $V_o = V_2 = -\frac{V_I}{2}$

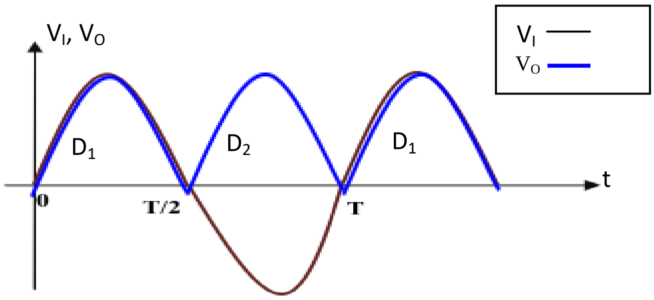


Figure 3-32 : Output Voltage Waveform of a Center-Tapped Full-Wave Rectifier

The output voltage is determined by the **turns ratio (n)** of the transformer. If the transformer turns ratio is known, the **peak output voltage** of a full-wave rectifier can be calculated using the following equation.

$$V_{OUT} = \frac{nV_{INP}}{2} \qquad (3.19)$$

Where n is number of turns in the secondary divided by the number of turn primary

B-The Bridge Rectifier

Another method of performing full-wave rectification, without the need for a center-tapped transformer, is to use four diodes arranged in a bridge circuit (Figure 3-33).

✓ **Operating principle**

Assumption: We assume that the diode is ideal ($V_0=r_d=0$) (Figure 3-34).

✓ **for the positive half-cycle** D_1 and D_3 conduct, while D_2 and D_4 are reverse-biased (blocked).

✓ **for the positive half-cycle** D_2 and D_4 conduct, while D_1 and D_3 are reverse-biased (blocked).

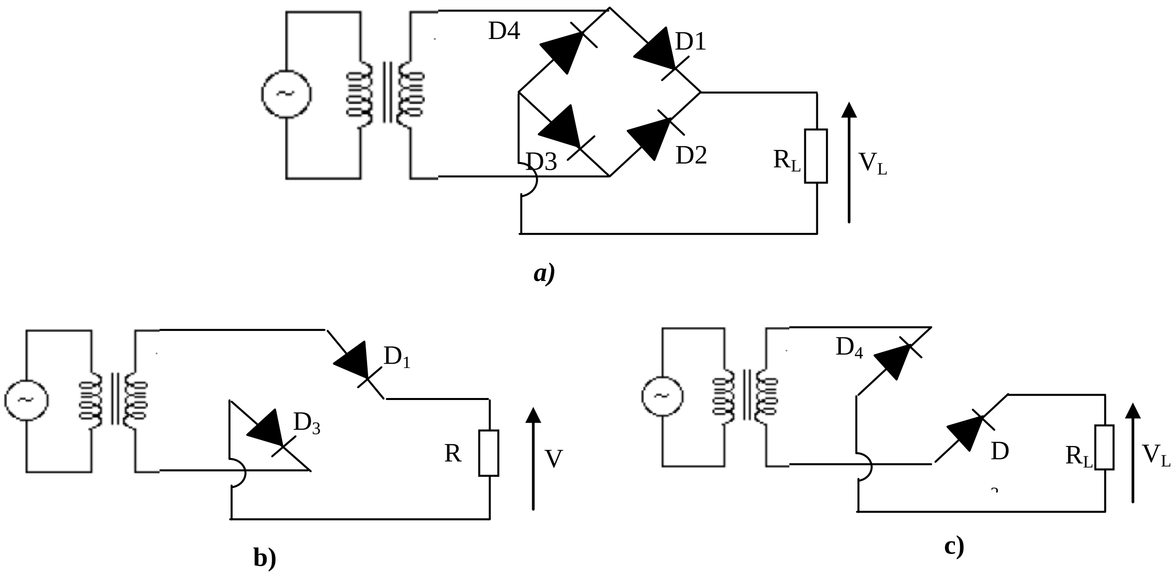


Figure 3-33 : (a) Bridge rectifier; (b) equivalent circuit for positive half-cycle; (c) equivalent circuit for negative half-cycle;

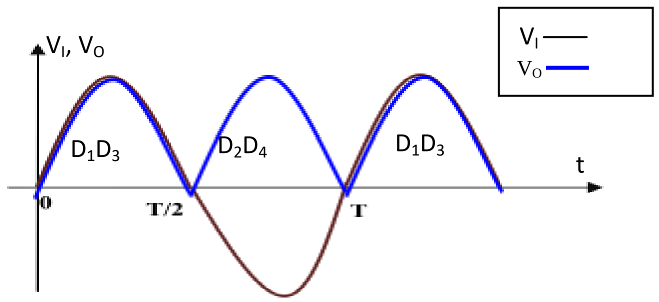


Figure 3-34 : Output Waveform of Full-Wave Bridge Rectifier

3.17.2 The Average Value (DC)

The average value of a periodic function with period T is given by

$$\overline{V}_{moy} = \frac{1}{T}\int_0^T V_S dt \tag{3.20}$$

$$V_O = V_{Imax} \sin \omega t \tag{3.21}$$

The average Value for Half-Wave Rectifier

$$\overline{V}_{Omoy} = \frac{1}{2\pi}\int_0^{\pi} V_{IMax} \sin \omega t d\omega t \tag{3.22}$$

On pose $\omega t = \theta$

$$\bar{V}_{Omoy} = \frac{1}{2\pi}\int_0^{\pi} V_{IMax} \sin\theta d\theta \qquad (3.23)$$

$$\bar{V}_{Omoy} = \frac{V_{IMax}}{\pi} \qquad (3.24)$$

The **average value for the full-wave rectifier** (center-tapped or bridge)

From Eq (3.6)

$$\bar{V}_{Omoy} = \frac{1}{\pi}\int_0^{\pi} V_{IMax} \sin\omega t d\omega t \qquad (3.25)$$

On pose $\omega t = \theta$

$$\bar{V}_{Omoy} = \frac{1}{\pi}\int_0^{\pi} V_{IMax} \sin\theta d\theta \qquad (3.26)$$

$$= \frac{V_{IMax}}{\pi}\left[-\cos\theta\right]_0^{\pi} = \frac{V_{IMax}}{\pi}\left[+1-(-1)\right] \qquad (3.27)$$

$$\bar{V}_{Omoy} = \frac{2V_{IMax}}{\pi} \qquad (3.28)$$

3.17.3 The RMS value (effective value)

The Root-Mean-Squared value of the AC voltage

$$\bar{V}_{eff}^2 = \frac{1}{T}\int_0^{T} V_S^2(t)dt \qquad (3.29)$$

The **RMS value for the full-wave rectifier** (center-tapped or bridge)

$$\bar{V}_{eff}^2 = \frac{1}{2\pi}\int_0^{\pi} \left(V_{IMax} \sin\omega t\right)^2 d\omega t \qquad (3.30)$$

On pose $\omega t = \theta$

$$\bar{V}_{eff}^2 = \frac{1}{2\pi}\int_0^{\pi} \left(V_{IMax} \sin\theta\right)^2 d\theta \qquad (3.31)$$

$$= \frac{V_{IMax}}{2\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\theta t}{2} \right) d\theta \tag{3.32}$$

$$= \frac{V_{IMax}^{\;\;2}}{4\pi} \left(\int_0^{\pi} [\theta]_0^{\pi} - \frac{1}{2} [\sin 2\theta]_0^{\pi} \right) \tag{3.33}$$

$$= \frac{V_{IMax}^{\;\;2}}{4} \tag{3.34}$$

$$V_{eff} = \frac{V_{IMax}}{2} \tag{3.35}$$

The **RMS value for the full-wave rectifier** (center-tapped or bridge)

From Eq (3.16)

$$\bar{V}_{eff}^{2} = \frac{1}{\pi} \int_0^{\pi} (V_{IMax} \sin \omega t)^2 \, d\omega t \tag{3.36}$$

On pose $\omega t = \theta$

$$\bar{V}_{eff}^{2} = \frac{1}{\pi} \int_0^{\pi} (V_{IMax} \sin \theta)^2 \, d\theta \tag{3.37}$$

$$= \frac{V_{IMax}}{\pi} \int_0^{\pi} \left(\frac{1 - \cos 2\theta t}{2} \right) d\theta \tag{3.38}$$

$$= \frac{VI_{sMax}^{\;\;2}}{2\pi} \left(\int_0^{\pi} [\theta]_0^{\pi} - \frac{1}{2} [\sin 2\theta]_0^{\pi} \right) \tag{3.39}$$

$$= \frac{V_{IMax}^{\;\;2}}{2} \tag{3.40}$$

$$V_{eff} = \frac{V_{IMax}}{\sqrt{2}} \tag{3.41}$$

3.17.4 Form Factor

Form factor (F.F) is defined as the ratio between RMS load voltage and average load voltage. The form factor of the half wave rectifier is as:

$$F = \frac{RMS}{evergeValue} \tag{3.42}$$

The form factor of a Half-wave rectified voltage

$$F = \frac{V_{IMax}}{2}\frac{\pi}{V_{IMax}} = 1.57 \tag{3.43}$$

The form factor of a Full-Wave rectified voltage :

$$F = \frac{V_{IMax}}{\sqrt{2}}\frac{\pi}{2V_{IMax}} = \frac{\pi}{2\sqrt{2}} = 1.11 \tag{3.44}$$

3.17.5 Power supply filter and regulators

A power supply filter ideally removes fluctuations in the output voltage of a half-wave or full-wave rectifier, producing a constant DC voltage level. In most power supply applications, the standard 50 Hz or 60 Hz AC line voltage must be converted into an approximately steady DC voltage.

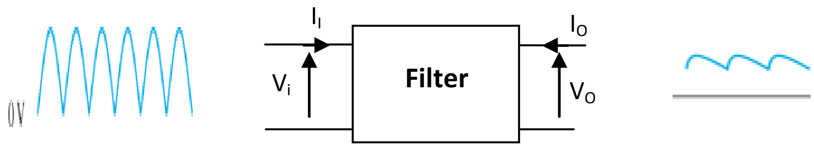


Figure 3-35 : Power supply filtering

3.17.5.1 Capacitor-Input Filter

A half-wave rectifier using a capacitor-input filter is illustrated in Figure 3-36.

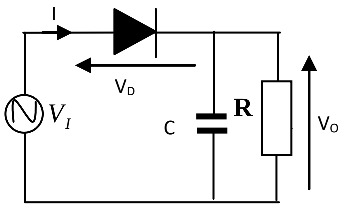


Figure 3-36 : Filtering the Output of a Rectifier

The shape of the voltage across the load R_L after filtering is shown in Figure 3-38.

1st Case: when the input voltage $V_I=0$

$\grave{a}\, t = 0 : V_I = 0 \Rightarrow V_C = 0$

2nd Case: when the input voltage $V_I > 0$

The input voltage increases $t \in \left[0, \frac{T}{4}\right]$ The diode becomes conductive, allowing the capacitor to charge rapidly with the circuit's time constant $\tau = r_d C$

3rd Case: At $t = t_1 = \frac{T}{4}$, that instant, the capacitor is charged to its maximum capacity, that is to say $V_C = V_{\max}$,

4th Case When the input voltage starts to decrease. The diode is reverse-biased, and the capacitor discharges slowly through the load R_L with a discharge time constant equal to $\tau = R_C C$.

5th Case. At this instant, the voltage V increases positively, the diode conducts, and the capacitor charges again

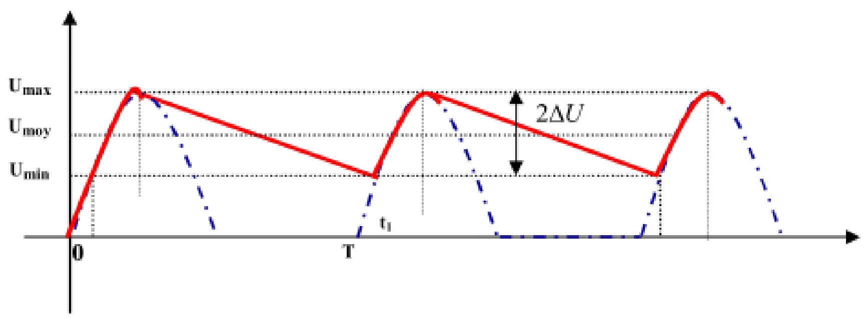


Figure 3-37 : Filter output is a dc voltage with small ripple

Note:

If the value of **C**, **R**$_L$, or both increases, the discharging time also increases, resulting in a smoother DC output. For very large values, the capacitor hardly discharges and behaves like a constant voltage source equal to the load voltage.

- **The ripple factor**

Ripple voltage is the fluctuation in the capacitor's output voltage caused by its periodic charging and discharging.

$$\tau = \frac{V_{rpp}}{V_{DC}} \quad (3.45)$$

Where

Vr(pp): is the peak-to-peak ripple voltage

V_{DC}: is the dc (average) value of the filters output voltage,

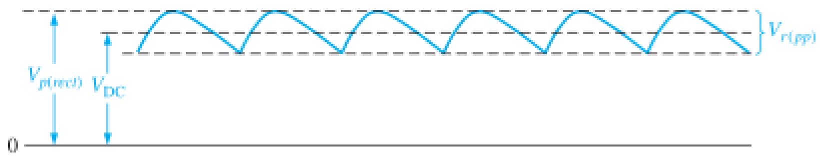


Figure 3-38 : Vr and VDC determine the ripple factor.

3.17.6 Stabilization

Stabilizing a ripple voltage consists of obtaining a practically constant voltage. This function can be achieved by a **Zener diode**

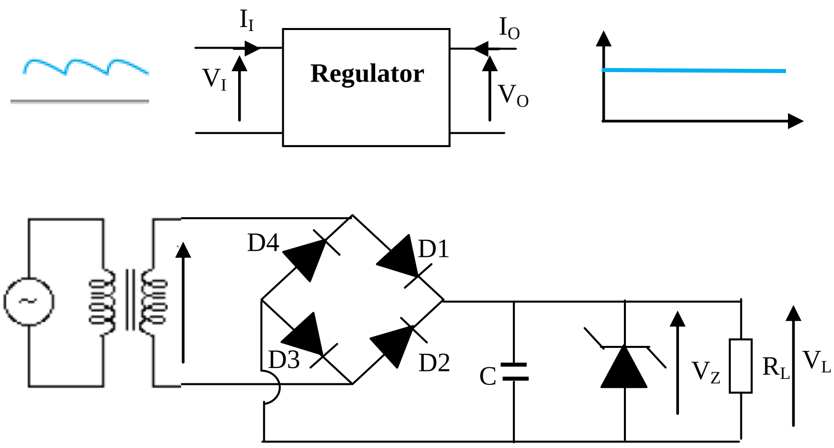


Figure 3-39 : Voltage Regulators

3.17.6.1 What is Zener Diode?

A **Zener diode** is a silicon p–n junction component specifically designed to operate in the **reverse breakdown region.** The key to zener diode operation is that, when a diode reache reverse breakdown, its voltage remains almost constant even though the current change drastically.

A major application for zener diodes is a type of voltage regulator for providing stable reference voltage for use in power supplies, voltmeters, and otter instruments

3.17.6.2 Symbol of zener diode

Figure 3-40 shows the Symbol of Zener diode

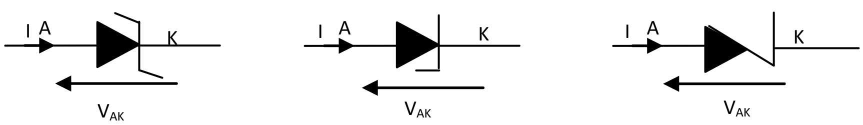


Figure 3-40 : Symbol of Zener diode

3.17.6.3 Characteristics of Zener Diode

The Zener diode has three regions of operations. Each region has it own approximation model. In the **forward-biased region**, the diode operates like a normal diode with a small forward voltage drop. In the **reverse-biased region**, only a very small leakage current flows. In the **Zener breakdown region**, the diode maintains an almost constant voltage (V) independent of the current.

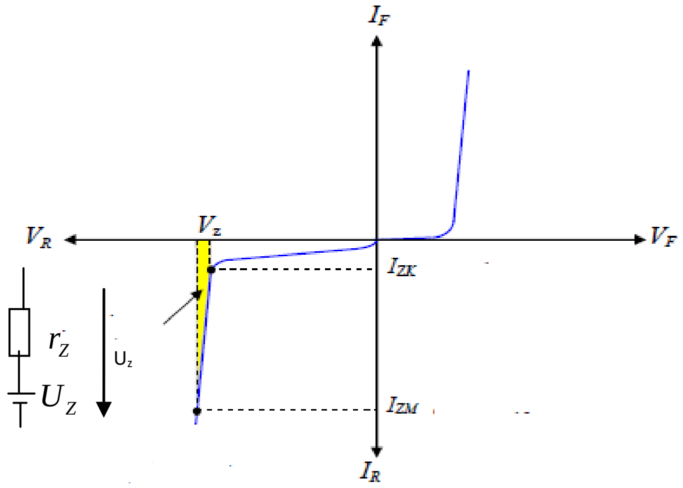


Figure 3-41 : Zener Diode Current–Voltage (I–V) Characteristic

The use of the Zener diode as a regulator is so common that three conditions surrounding the analysis of the basic Zener regulator are considered:

1 Fixed load and fixed supply voltage.

2 Fixed supply voltage and variable load.

3 Variable supply voltage and fixed load..

3.17.6.4 Fixed load and fixed supply voltage

The most basic Zener diode voltage regulator circuit is illustrated in Figure 3-42. In this configuration, the DC input voltage as well as the load resistor are considered fixed. To simplify the study of this circuit, the analysis can be carried out in two main steps.

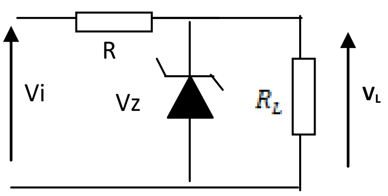


Figure 3-42 : Basic Zener regulator

1- To identify the operating state of the Zener diode, first remove it from the circuit and determine the voltage that appears across the open-circuit terminals.

By applying the Voltage Divider Rule (VDR) to circuit of Figure 3-42 results in the network of Figure 3-43, we obtain:

$$V = V_L = \frac{R_L}{R_L + R} V_i \tag{3.46}$$

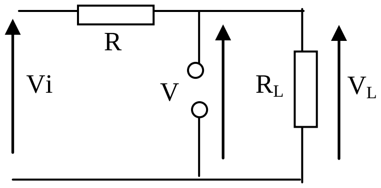


Figure 3-43 : Analyzing the operating state of the Zener diode

If $V \geq V_Z$, the Zener diode is ON state, and $V_L = V_Z$

If $V < V_Z$, the Zener diode is in the OFF state, and it can be replaced by its open-circuit equivalent in the analysis.

Substitute the Zener diode with its appropriate equivalent model and then examine the circuit to find the desired unknown values.

$$V = V_L = \frac{R_L}{R_L + R} V_i \tag{3.47}$$

For the circuit in Figure 3-42, when the Zener diode is in the "ON" state, the network becomes equivalent to that shown in Figure 3-44 Because the voltages across parallel components are equal, it follows that

$$V_L = V_Z \tag{3.48}$$

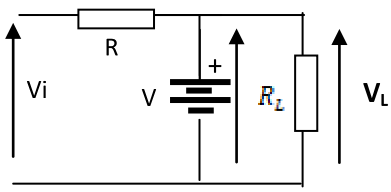


Figure 3-44 : Substituting the Zener equivalent for the "on" situation

The current through the Zener diode can be found using **Kirchhoff's Current Law (KCL)**.

$$I_R = I_Z + I_L \tag{3.49}$$

and

$$I_Z = I_R - I_L \tag{3.50}$$

Where

$I_L = \frac{V_L}{R_L}$ and $I_R = \frac{V_R}{R} = \frac{V_I - V_Z}{R}$

3.17.6.5 Fixed supply voltage and variable load

Because of the Zener voltage V_Z, only a limited range of resistor values and consequently load currents will keep the Zener diode in the "ON" state. If the load resistance R_L is too low, the voltage across it V_L will fall below V_Z , and the Zener diode will switch to the "OFF" state

To find the **minimum value of the load resistance R_L** that will cause the Zener diode in Fig. 3.43 to start conducting, determine the value of R_L that produces a **load voltage V_L** equal to the **Zener voltage V_Z** In other words, calculate RL under the condition that

$$V_Z = V_L = \frac{R_L}{R_L + R} V_i \tag{3.51}$$

Solving for R_L, we obtain

$$R_{L\min} = \frac{RV_Z}{V_i + V_Z} \tag{3.52}$$

Any load resistance R_L greater than the value obtained from Eq. (3.52) will guarantee that the Zener diode is in the **ON state**, allowing it to be replaced by its equivalent **Zener voltage source V_Z**. The condition given by Eq. (3.52) therefore defines the **minimum value of R_L** and, consequently, determines the **maximum load current I_L** as follows:

$$I_{L\min} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L\min}} \tag{3.53}$$

Once the diode enters the **ON state**, the voltage across the resistor (R) remains constant at :

$$V_R = V_i - V_Z \tag{3.54}$$

and I_R remains fixed at

$$I_R = \frac{V_Z}{R} \tag{3.55}$$

The Zener current

$$I_R = I_R - I_L \tag{3.56}$$

This results in a minimum Zener current I_Z when the load current I_L is at its maximum, and a maximum Zener current I_Z when I_L is at its minimum, since I_R remains constant. Because I_Z is limited to its maximum rating I_{ZM}I as specified in the datasheet, this restriction affects the permissible range of R_L and, consequently, I_L. By substituting I_{ZM} for I_Z, the minimum load current I_L is established as:

$$I_{L\min} = I_R - I_{ZMax} \tag{3.57}$$

and the maximum load resistance as

$$R_{LMax} = \frac{V_Z}{I_{L\min}} \tag{3.58}$$

3.17.6.6 Variable supply voltage and fixed load

For a given fixed value of R_L in Figure 3-43, the input voltage Vi must be high enough to make the Zener diode conduct. The **minimum turn-on voltage**, Vimin, is calculated as:

$$V_Z = V_L = \frac{R_L}{R_L + R} V_i \tag{3.59}$$

and

$$V_{i\min} = \frac{(R_L + R)V_Z}{R_L} \tag{3.60}$$

The **maximum input voltage V_i** is limited by the **maximum Zener current I_{ZM}**. Since

$$I_{RMax} = I_{ZMax} + I_L \tag{3.61}$$

Since I_L is fixed at V_Z R_L and I_{ZM} is the maximum value of I_Z , the maximum V_i is defined by

$$V_{IMax} = I_{RMax} R + V_Z \tag{3.62}$$

3.17.7 The Clipper

A **clipper** is an electronic circuit designed to cut off either the positive or negative portion of a waveform. Such processing is applied in signal shaping, circuit protection, and communication systems.

3.17.7.1 Types of clipper

Figure 3- 45 shows types of Clippers

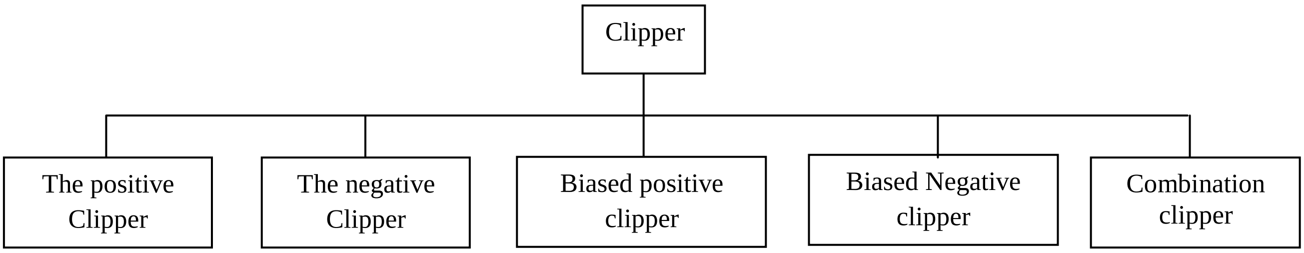


Figure 3-45 : Types of Clippers

a- The positive clipper :

Figure 3-46.a shows a positive clipper. The circuit removes all the positive parts of the input signal. This is why the output signal has only negative half-cycles.

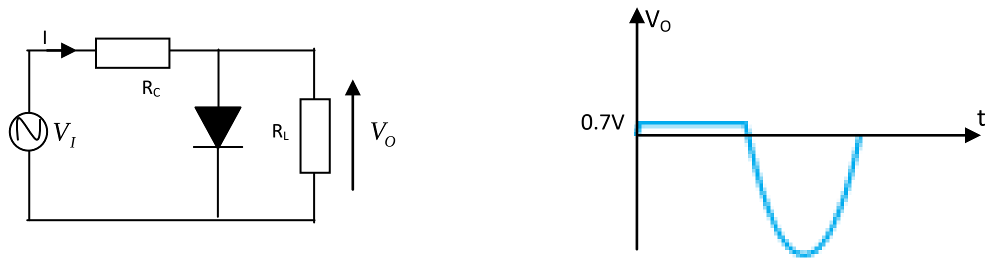


Figure 3-46 : The positive clipper

As the input voltage goes positive, the diode becomes forward biased and conducts current. Point A is limited to +0.7 V when the input voltage exceeds this value (Figure 3-46.b.

$$V_D = 0.7V = V_O \tag{3.63}$$

The ouput voltage is determined by the voltage divider formed by R_S and the load resistor, R_L, as follows:

$$V_O = \frac{R_L}{R_L + R_S} V_I \tag{3.64}$$

If R_S is small compared to R_L, Then

$$V_O \cong V_I \tag{3.65}$$

b- The Negative clipper :

When the diode's polarity is reversed, as in Figure 3-47(b), the negative part of the input voltage is clipped off. When the diode is forward-biased during the negative part of the input volt age, point A is held at - 0.7 V by the diode drop. When the input voltage goes above - 0.7 V, the diode is no longer forward-biased; and a voltage appears across R_L propor tional to the input voltage.

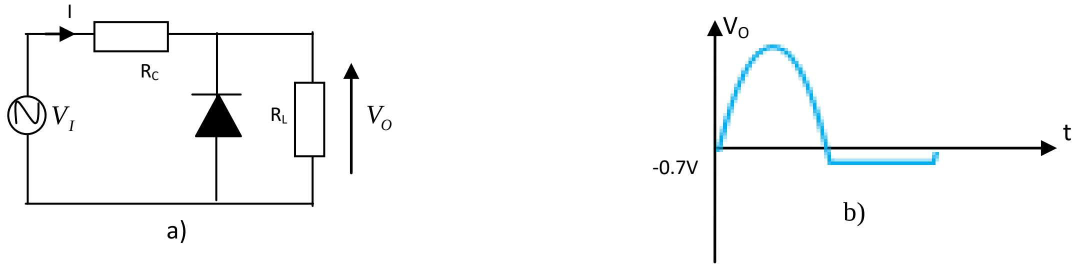


Figure 3-47 : The Negative clipper

c- The Combination clipper :

If we connected two diodes in inverse parallel as shown, then both the positive and negative half cycles would be clipped as diode D_1 clips the positive half cycle of the sinusoidal input waveform while diode D_2 clips the negative half cycle.

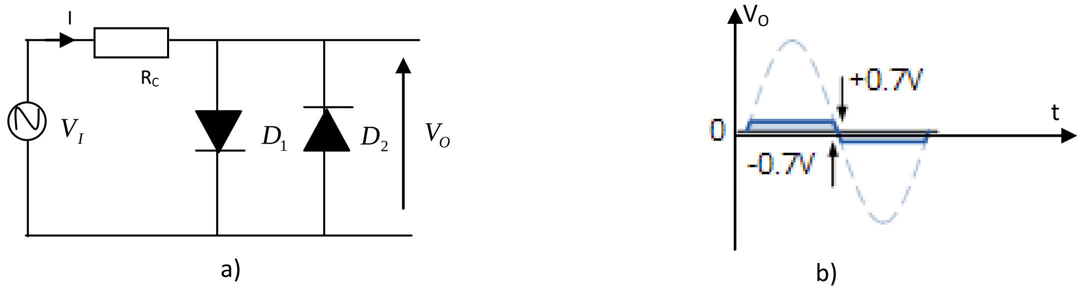


Figure 3-48 : The Combination clipper

d- Biased positive clipper

To clamp a voltage to a specified positive level, the diode D_1 and the bias voltage need to be connected as illustrated in Figure 3-50. In this configuration, the voltage at point A must drop above $+V_{1BIAS}+0.7$ V in order to forward-bias the diode. Once this threshold is reached, the diode conducts and the limiting (clipping) action begins

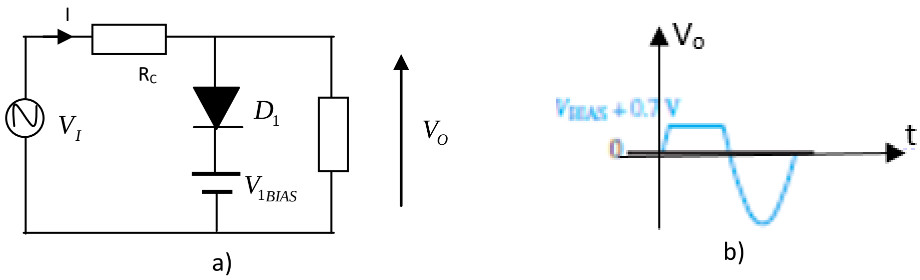


Figure 3-49 : Biased posit[illegible]

e- Biased negative clipper

To clamp a voltage to a specified negative level, the diode and the bias voltage need to be connected as illustrated in Figure 3-50. In this configuration, the voltage at point A must drop below $-V_{2BIAS}-0.7$ V in order to forward-bias the diode. Once this threshold is reached, the diode conducts and the limiting (clipping) action begins

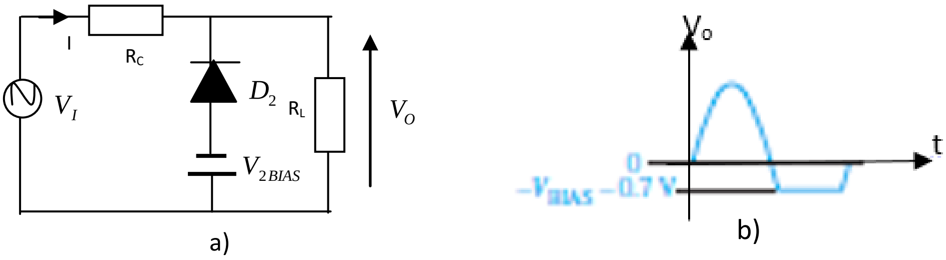


Figure 3-50 : Biased negative clipper

f-The Combination Baisd clipper

When the voltage at point *A* reaches $V_{BIAS}+ 0.7$ V, diode D_1 conducts and limits the waveform to $V_{BIAS}+ 0.7$ V. Diode D_2 does not conduct until the voltage reaches $-V_{BIAS}- 0.7$. Therefore, positive voltages above $V_{BIAS}+ 0.7$ V and negative voltages below $-V_{BIAS}- 0.7$ V are clipped off. The resulting output voltage waveform is shown in Figure 3-51.

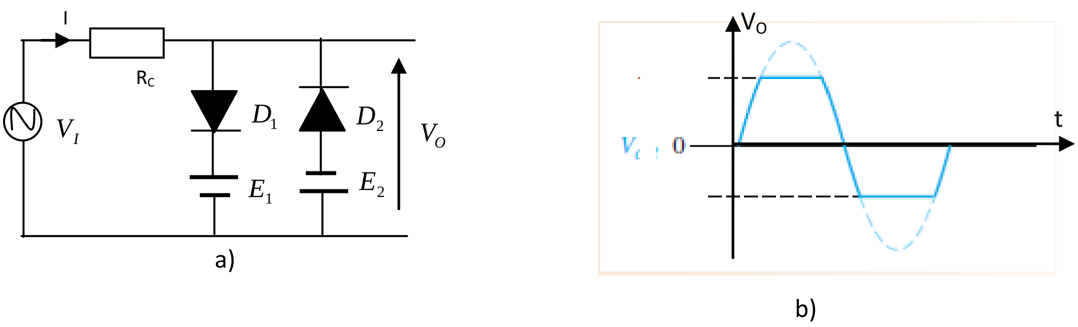


Figure 3-51 : The Combination biasd clipper

3.18 Special types of diodes

3.18.1 The Light emitting diode (LED)

Light emitting diode is a special type of diode or special form of PN junction, which converts electrical energy into light energy under forward biasing. The reverse bias operation of LEDs is avoided due to very low breakdown voltage.

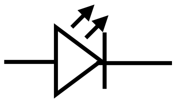
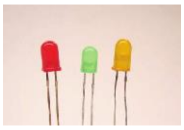



Figure 3-52 : The Light emitting diode (LED)

3.18.2 The photodiode

The **photodiode** is a device that operates in reverse bias, where is the reverse light current. The photodiode has a small transparent window that allows light to strike the pn junction. Photodiodes are widely used in various applications, such as **light detection, optical communication, Optical sensors, …**

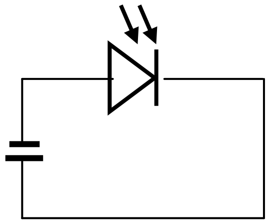


Figure 3-53 : The photodiodes

3.18.3 Varicap diode

A **varactor diode** (also called **varactor diode** or **tuning diode**) is a p-n junction diode whose capacitance changes with the applied reverse voltage. It functions exclusively in reverse bias, where it behaves like a **variable capacitor**

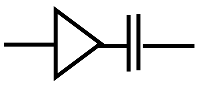


Figure 3-54 : The Varicap diode

3.19 Glossary

Français	**English**	العربية
Diode	diode	صمام ثنائي
Conducteur	Conductor	ناقل
Isolant	insulator	عازل
Semi-conducteur	Semiconductors	شبه نواقل
Bande d'énergie	Energy Bands	حزم الطاقة
Bande de valence	Valence band	حزمة تكافؤ
Bande de conduction	Conduction band	حزمة توصيل
Bande interdite	band Forbidden	حزمة ممنوعة
Gap d'enérgie	Energy Gap	الفجوة الطاقية
S-C Intrinsèque	S-C intrinsic	أشباه الموصلات نقية
S-C Extrinsèque	S-C Extrinsic	أشباه الموصلات ذات شوائب
Dopage	Doping	تطعيم
éléments trivalents	impuritiesTrivalent	عناصرثلاثية التكافؤ
éléments pentavalents	Pentavalent impurities	عناصرخماسية التكافؤ
Jonction PN	PN junction	وصلة PN
Redressement	rectifier	التقويم
Filtrage	filter	الترشيح
Régulation	Regulator	التثبيث
Diode Varicap	Varactor Diode	الثنائى السعوى
Les diodes électroluminescentes	Light-Emitting Diode	الثنائي البعث للضوء
Les photodiodes	Photodiode	الثنائى الضوئى

DIODE

Exercises

Exercise 3.1: Diode Approximations

Consider the circuit in Figure 3-55:

Calculate the **voltage and current values** for the three cases 1.2 and 3

1-Ideal diode model

2-The Practical Diode Model $(V_0 = 0.3V)$

3-The Complete Diode Model $(V_0 = 0.3V \; and \, r_d = 10\Omega)$

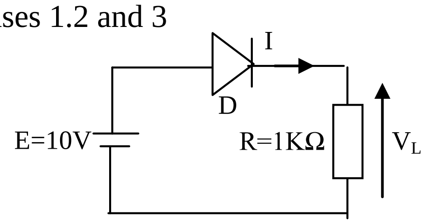


Figure 3-55 : Circuit for Exercise 03.1

Exercise 3.2: Diode caracteritic

An experimental measurement on a silicon diode produced the following table:

V_d (V)	0.58	0.6	0.7	0.75
I_d (A)	0.6	1	3	4

1- Plot the characteristic of this diode.
2- What is the value of the dynamic resistance r_d for $0.6 \prec I(A) \prec 3$?
3- Determine the threshold voltage.
4- Give the equivalent electrical circuit of this diode in the forward direction.
5- Knowing that the maximum dissipated power is $P_{max} = 3W$, calculate $V_{max} \; and \, I_{max}$
6- Now suppose that this diode is inserted into the circuit shown below. Determine the value of E so that the load line passes through the point $M(0V, 4A)$., then deduce the operating point P after having plotted (the load line).

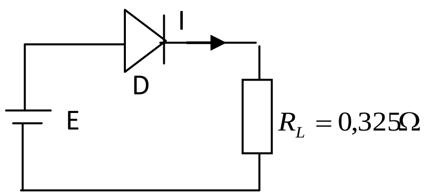


Figure 3-56 : Circuit for Exercise 03.2

Exercise 03.3: Combination Clipper

Consider the following circuit 3.57 The diodes are assumed to be ideal.

$V_{in} = 15\sin\omega t;\ E_1 = 10V\ and\ E_2 = 5V$

Analyze the operation of the assembly and plot

the graph of the voltage Vs as a function of time

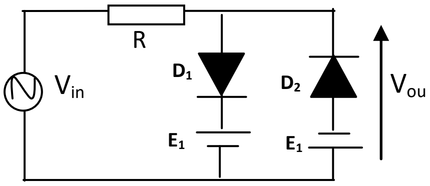


Figure 3-57 : Circuit for Exercise 03.3

Exercise 03.4: V_i and R_L fixed.

(a) Determine V_L, I_L, I_Z, and I_R for the network Fig. 3.58 if R_L = 180Ω

(b) Repeat part (a) if R_L = 470Ω

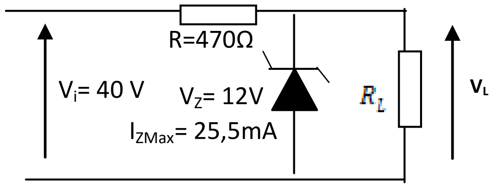


Figure 3-58 : Circuit for Exercise 03.4

Exercise 03.5: V_i and R_L Variable.

For the network shown, determine the range of R_L, and I_L result in V_{RL} being maintained at 12

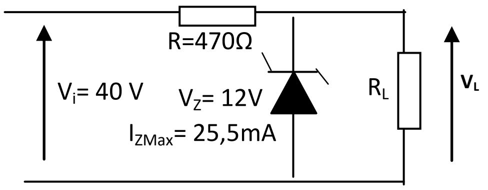


Figure 3-59 : Circuit for Exercise 03.5

Exercise 03.6: Fixed R_L, Variable V_i

For the given network, determine the range of Vi that will maintain V_L at 8V and not exceed the maximum power rating of the Zener diode.

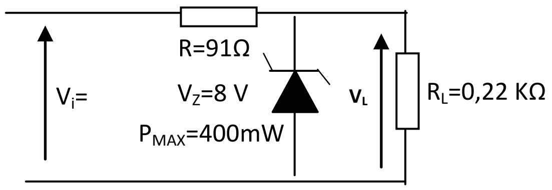


Figure 3-60 : Circuit for Exercise 03.6

DIODE

Solutions

Exercise 3.1: Diode Approximations

1. Using the **ideal diode model**, determine the **load voltage** and **load current** for the circuit shown in **Fig. 3-55a** as follows:

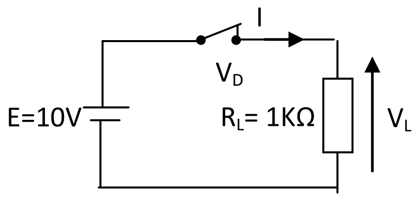


Figure 3-55.a

Since the diode is forward-biased, it behaves like a **closed switch**. If you imagine replacing the diode with a closed switch in the circuit, it becomes clear that **the entire source voltage is applied across the load resistor**

$V_L = E = 10V$

Applying Ohm's law, we obtain the load current as

$$E = R_L I_L \Rightarrow I_L = \frac{E}{R_L} = \frac{10}{1K\Omega} = 10mA$$

2- Apply the **second approximation** to compute the load voltage and load current, shown in Figure. 3-55.b

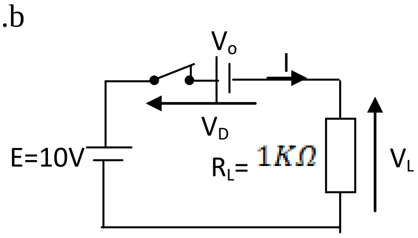


Figure 3-55.b

With the diode in forward bias, it is equivalent to a 0.7 V voltage source, so the load voltage is the source voltage minus this drop

$V_L = E - V_D = 10 - 0.7 = 9{,}3V$

Applying Ohm's law, we obtain the load current as

$$E = R_L I_L \Rightarrow I_L = \frac{V_L}{R_L} = \frac{9{,}3}{1K\Omega} = 9{,}3\,mA$$

1- Apply the **thrid approximation** to compute the load voltage and load current, shown in Figure. 3-55.c

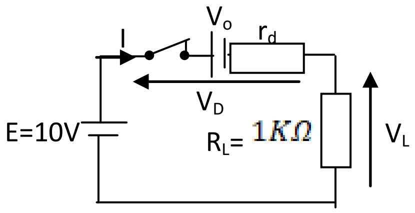


Figure 3-55.c

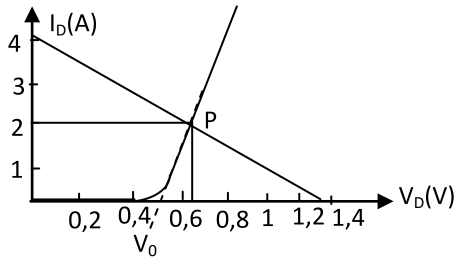
During forward bias, the diode may be represented by a closed switch together with a series barrier potential V_o and a small forward dynamic resistance rd.

Applying Ohm's law, we obtain the load current as

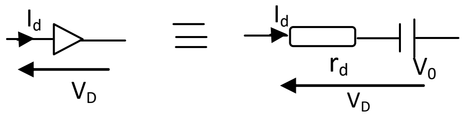
$$E = (R_L + r_d)I_L + V_O \Rightarrow I_L = \frac{E - V_L}{r_d + R_L} = \frac{10 - 0{,}7}{10 + 1K\Omega} = 9{,}2\,mA$$

Exercise 3.2: Diode caracteritic

1. Plotting the characteristic curve



2. Dynamic resistance: $rd = \frac{\Lambda U}{\Delta I} = \frac{0{,}7 - 0{,}6}{3 - 1} = 0{,}05\Omega$
3. Graphical determination of the threshold voltage: $V_0 = 0{,}55V$
4. Equivalent model of the diode



5. The value of the maximum voltage and the maximum curren

$$P_{\max} = V_{D\max} I_{\max} = (rdI_{\max} + V_d)I_{\max}$$

$$rdI_{\max}^2 + V_d I_{\max} - P_{\max} = 0$$

$$5.10^{-2} I_{\max}^2 + 0{,}55 I_{\max} - 3 = 0$$

Solving this equation gives two current solutions, but only the positive value is kept.

$$I_{\max} = 4A \Rightarrow V_{\max} = 0{,}75V$$

1. Load line equation

$$E = RI_D + V_D \Rightarrow I_D = \frac{E}{R} - \frac{V_D}{R} \qquad V_D = 0 \Rightarrow I_D = \frac{E}{R}\ donc E = RI_D = 0{,}325 \times 4 = 1{,}3V$$

The load line passes through the points… $M_1(0V, 4A).et\, M_2(1{,}3V, 0A)$

Exercise 03.3: Combination Clipper

When the voltage at point A reaches +10 V, diode D_1 conducts and limits the wave form to +10 V. Diode D_2 does not conduct until the voltage reaches -5V. Therefore, positive voltages above +10 V and negative voltages below -5V are clipped off. The resulting output voltage waveform is shown in Figure 3-57

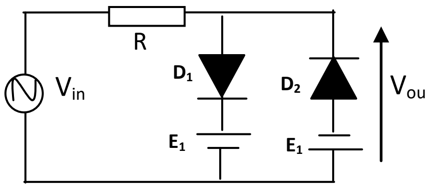


Figure 3-57

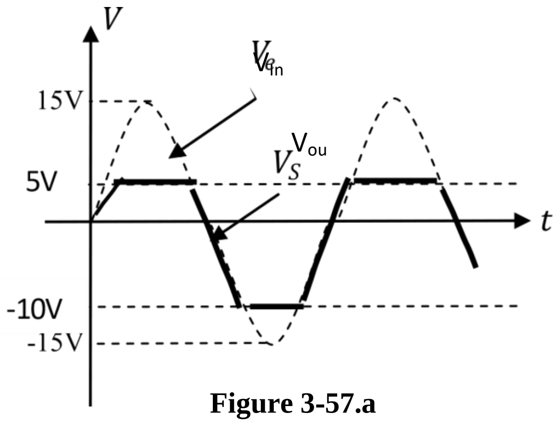


Figure 3-57.a

Exercise 03.5: V_i and R_L fixed.

a. We repaint the network in accordance with the recommended process, as illustrated in Figure 3-58.

Using Eq. (3.46) yields

$$V = V_L = \frac{R_L}{R_L + R} V_i = \frac{180}{180 + 220} 20 = 9V$$

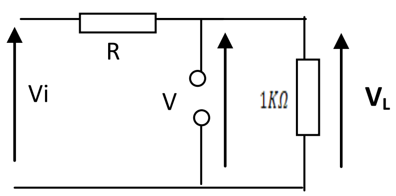


Figure 3-58.a: Calculating V for the regulator in Figure 3.58

The characteristics of Figure 3-58.b show that the diode is in the "off" state since V = 9V is less than V_Z = 10 V. Substituting the open-circuit equivalent yields the same network as shown in Figure 3-58a, where we find that.

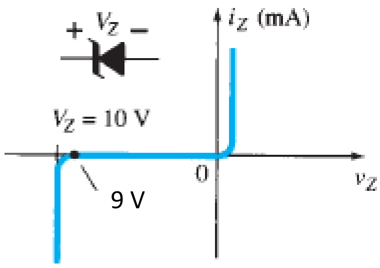


Figure 3-58.b: The operating point corresponding to the network of Fig. 3-58.a

$$V_L = V = 9V$$

$$V_R = V_i - V_L = 20 - 9 = 11V$$

$$I_Z = 0$$

And $P_Z = I_Z V_Z = 0 \times 10 = 0W$

- $R_L = 470\Omega$

  Applying Eq. (3.46), we find

$$V = V_L = \frac{R_L}{R_L + R} V_i = \frac{470}{470 + 220} 20 = 13{,}62V$$

The network shown in Figure 3-58.c is the result of the diode being in the "on" state since V=13,62 V is greater than V_Z 10 V. When Eq. (3.46) is applied,

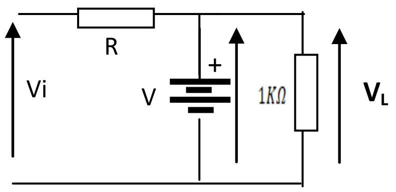


Figure 3-58.c: Network of Fig. 3.58 operation in the "on" state.

$$V_L = V = 10V$$

$$V_R = V_i - V_L = 20 - 10 = 10V$$

$$V_L = V = 9V$$

$$I_L = \frac{V_L}{R_L} = \frac{10}{470} = 0{,}021A$$

$$I_R = \frac{V_R}{R} = \frac{10}{220} = 0{,}045A$$

$$I_Z = I_R - I_L = 0{,}045 - 0{,}021 = 0{,}024A$$

The power dissipated is

$$P_Z = I_Z V_Z = 0{,}024 \times 10 = 240mW$$

which is less than the specified P_{ZM} =400 mW.

Exercise 3.5: V_i fixed and R_L variable

To determine the minimum load resistance of the regulator in the figure below that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is:

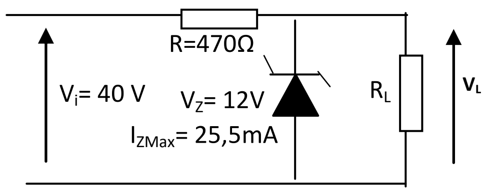


Figure 3-59

$$V_L = \frac{R_L}{R_L + R} V_i \Rightarrow V_L (R_L + R) = V_i \ R_L$$

$$(V_L - V_i) R_L = RV_L$$

$$R_{L\min} = \frac{RV_L}{V_L - V} = \frac{470}{40 - 12} 12 = 201\Omega$$

It means any load resistance greater than R_{Lmin} will make the diode ON.

R_{LMax}= ?

The voltage across the resistor R is:

$$V_R = V_i - V_L = 40 - 12 = 28V$$

The magnitude of I_R is:

$$I_R = \frac{V_R}{R} = \frac{28}{470} = 0{,}0595A$$

Then the Zener current:

$$I_{ZMax} = I_R - I_{L\min} \Rightarrow I_{L\min} = I_R - I_{ZMax} = 0{,}0595 - 0{,}0255 = 0{,}034A$$

and the maximum load resistance as:

$$R_{LMax} = \frac{V_L}{I_{L\min}} = \frac{12}{0{,}034} = 352\Omega$$

Plot of **$V_L = f(R_L)$** appears in Figure 3-59a and for V_L versus I_L in Figure 5-59.b .

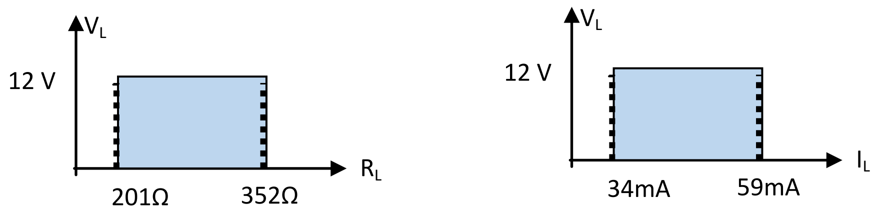


Figure 3-59.a: Variation of V_L with R_L and V_L for the regulator of figure 3-59

Exercise 03.6: Fixed R_L, Variable V_i

Applying Eq. (3.60), we find (fiure 3-60)

$$V_{i\min} = \frac{(R_L + R)V_Z}{R_L} = \frac{(0{,}22K\Omega + 91)8}{0{,}22K\Omega} = 11{,}3V$$

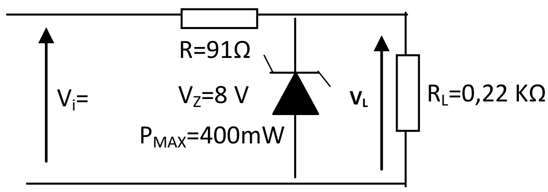


Figure 3-60

$$I_L = \frac{V_L}{R_L} = \frac{8}{0{,}22K\Omega} = 36{,}36mA$$

Applying Eq. (3.61), we find : $I_{RMax} = I_{Z\max} - I_L$

$$I_{ZMax} = \frac{P_{Max}}{V_Z} = \frac{400mA}{8} = 50mA$$

$$I_{RMax} = I_{Z\max} + I_L = 50mA + 36{,}36mA = 86{,}36mA$$

Applying Eq. (3.62), we find

$$V_{IMax} = I_{RMax}R + V_Z = (86{,}36mA)91 + 8 = 15{,}85V$$

The variation of V_L with V_i

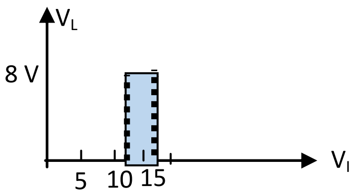


Figure 3.60.a: Variation of V_L with V_I of figure 3.60

Chapter 04

BIPOLAR JUNCTION TRANSISTOR (BJT)

4 BIPOLAR JUNCTION TRANSISTOR (BJT)

Learning Objectives

By studying this chapter and completing the related exercises, you will be able to:

1. Understand the transistor effect and the basic operation of transistors.
2. Identify the different operating modes of a transistor, including cutoff, active, and saturation regions.
3. Analyze the network of static characteristics of transistors.
4. Understand transistor biasing techniques and their importance in circuit stability.
5. Determine and analyze the load line and quiescent point (Q-point) of transistor circuits.
6. Study the three basic transistor configurations: Common Emitter (CE), Common Base (CB), and Common Collector (CC).
7. Analyze the equivalent circuits of transistor amplifiers.
8. Calculate voltage gain, current gain, and power gain in transistor circuits.
9. Determine the input and output impedances of transistor amplifiers.
10. Study multistage low-frequency amplifiers under static and dynamic operating conditions.
11. Understand the role and operation of coupling capacitors and bypass capacitors in amplifier circuits.
12. Explore other transistor applications such as the Darlington configuration and transistor switching circuits.

4.1 What is a bipolar transior?

The transistor, derived from transfer-resistor, is a three terminal device whose resistance between two terminals is controlled by the third. The term bipolar reflects the fact that there are two types of carriers, holes and electrons which form the currents in the transistor. If only one carrier is employed (electron or hole), it is considered a unipolar device like field effect transistor (FET).

The BJT (bipolar junction transistor) is constructed with three doped semiconductor regions separated by two p-n junctions. The 3 regions are called **emitter**, **base**, and **collector.**

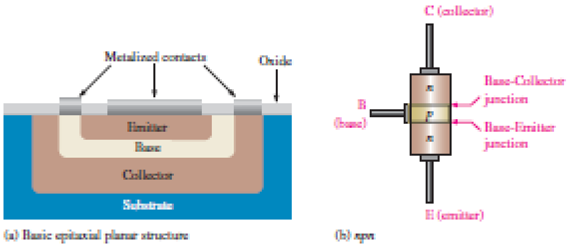


Figure 4-1 : Basic BJT construction

- **Emitter (E):** Heavily doped region that injects charge carriers (electrons or holes).
- **Base (B):** Thin and lightly doped region that controls the transistor's operation.
- **Collector (C):** Moderately doped region that collects carriers from the emitter.

4.2 Basic model of BJT

Figure 4-2 illustrates the schematic symbols for both NPN and PNP bipolar junction transistors

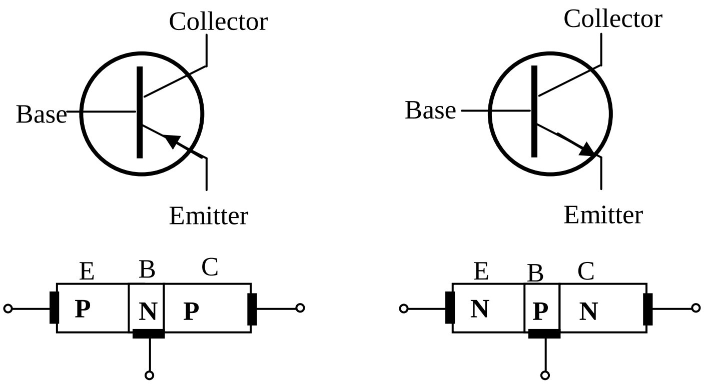


Figure 4-2 : Standard BJT (bipolar junction transistor) symbols

Note:

That emitter is shown by an arrow which indicates the direction of conventional current flow with forward bias

4.3 Basic BJT Operation

In order for a BJT to operate properly as an amplifier, the two pn junctions must be correctly biased with external dc voltages.

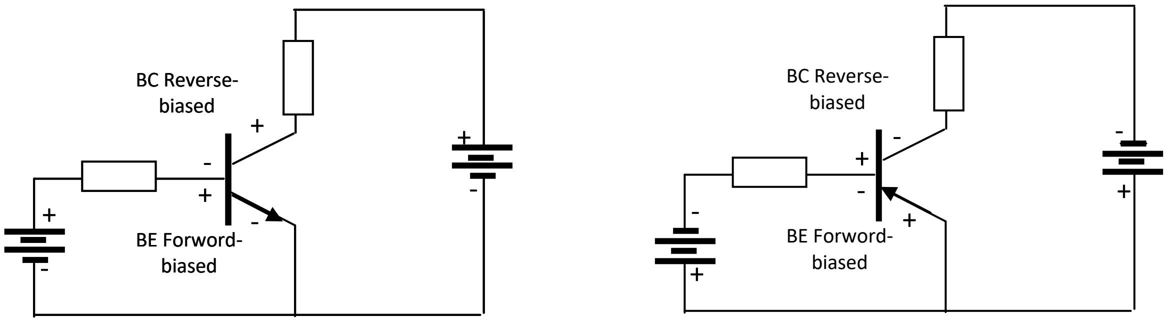


Figure 4-3 : Forward-Reverse bias of a BJT

Figure 4-3 shows a bias arrangement for both npn and pnp BJTs for operation as an amplifier. In both cases the base-emitter (BE) junction is forward-biased and the base-collector (BC) junction is reverse-biased. This condition is called **forward-reverse bias.**

- The heavily doped n-type emitter region has a very high density of conduction-band (free) electrons,
- These free electrons easily diffuse through the forward based BE junction into the lightly doped and very thin p-type base region
- A small percentage of the total number of free electrons injected into the base region recombine with holes and move as valence electrons through the base region and into the emitter region as hole current, indicated by the red arrows
- Most of the free electron that have entered the base do not recombine with holes because the base is very thin
- As the free electron move toward the reverse-biased BC junction, they are swept across into the collector region by the attraction of the positive collector supply voltage
- The emitter current is slightly greater than the collector current because of the small base current that splits off form the total current injected into the base region form the emitter

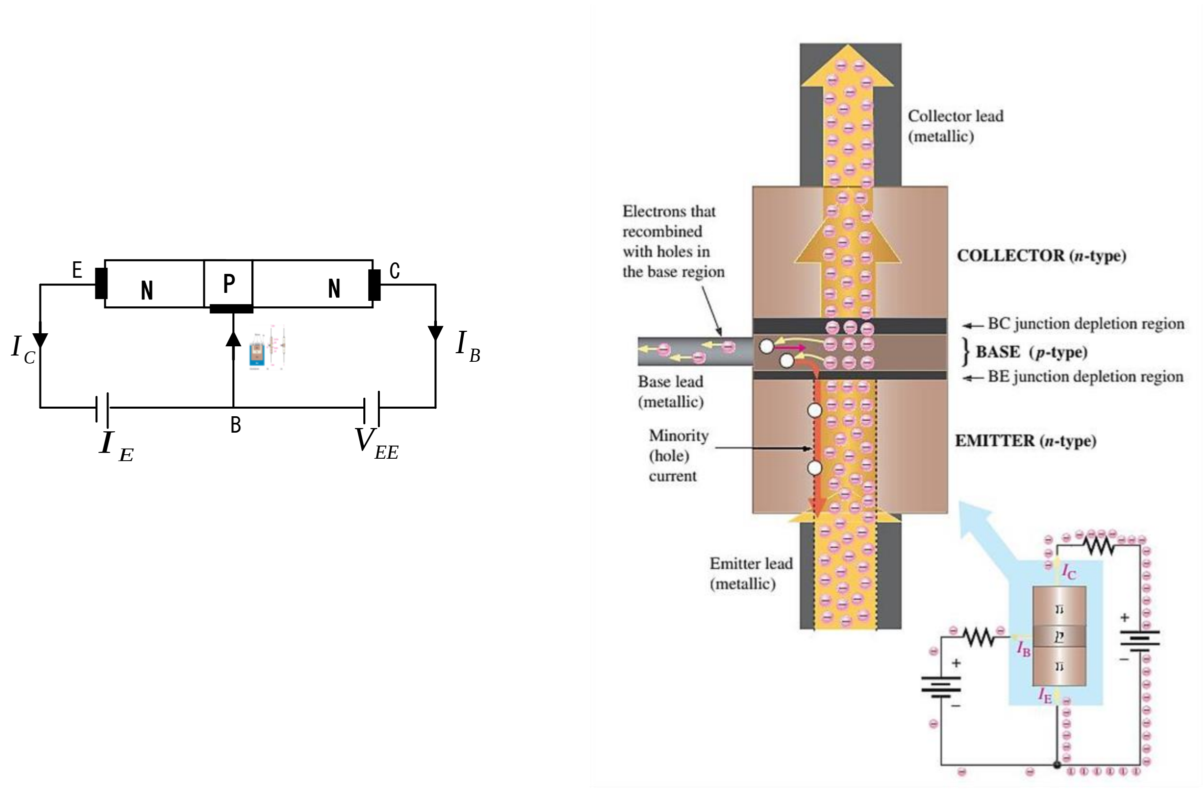


Figure 4-4 : Basic BJT Operation

4.4 Transistor Currents and voltages

Figure 4-5 shows a basic transistor bias circuit configuration, in which three DC currents and three DC voltages can be identified :

V_{BE}: dc voltage at base with respect to emitter

V_{CB}: dc voltage at collector with respect to base

V_{CE}: dc voltage at collector with respect to emitter

$$V_{CE} = V_{CB} + V_{BE} \tag{4.1}$$

$V_{BE} \cong 0.7\text{V for silicom and } 0.3\text{V for Germanium}$

I_B: dc base current

I_E: dc emitter current

I_C: dc collector current

$$I_E = I_C + I_B \tag{4.2}$$

Since the base current is so small, the collector current approximately equals the emitter current: $I_E = I_C$

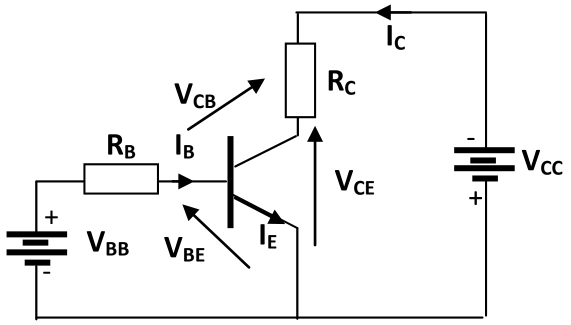


Figure 4-5 : BJT analysis

4.4.1 DC Beta (β_{DC})

The Beta of a transistor is defined as the ratio of the dc collector current to the dc base current:

$$\beta_{DC} = \frac{I_C}{I_B} \tag{4.3}$$

4.4.2 Alpha (α_{DC})

The dc alpha is defined as the dc collector current divided by the dc emitter current:

$$\alpha_{DC} = \frac{I_C}{I_E} \tag{4.4}$$

4.5 BJT analysis

Figure 4-6 shows a BJT analysis, in which two analysis DC analysis and AC analysis:

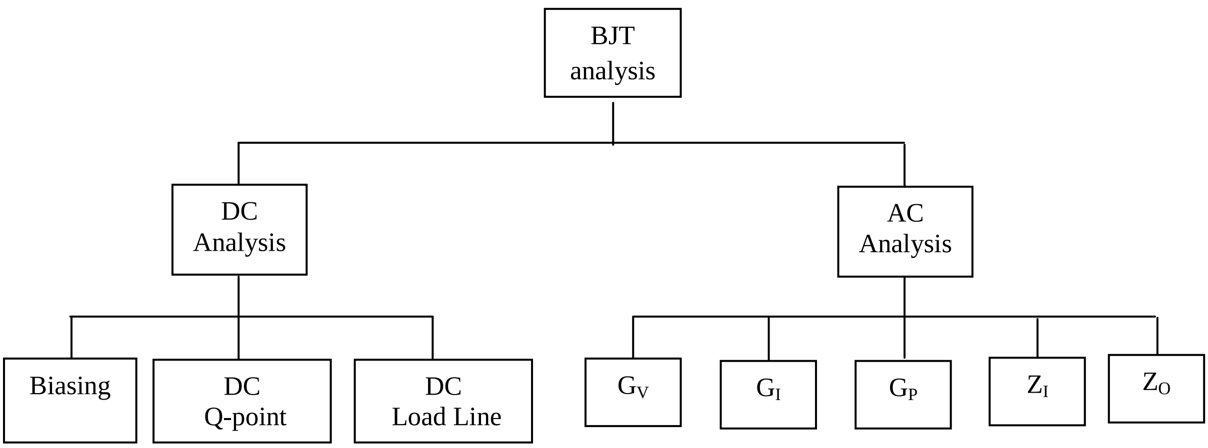


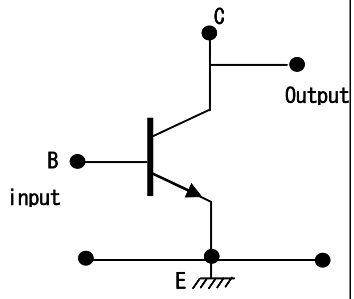
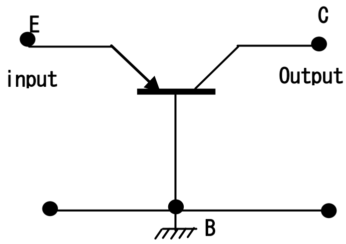
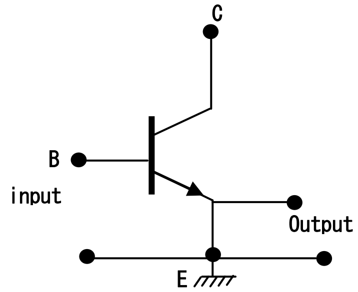
Figure 4-6 : BJT analysis

4.5.1 DC Analysis

4.5.1.1 Transistor configurations

Objective: Shows the transistor connection configurations and the difference between them

Table 4-1 : Transistor configuration

common emitter (CE)	common base (CB)	common collector (emitter follower) (CC)
		
Input : base Output :collector	Input : emitter Output :collector	Input : base Output :emitter

Note:

The term '**common**' refers to the component shared by both the input and output circuits, which is typically connected to ground

4.5.1.2 The Common Emitter (CE) Configuration.

Two sets of characteristics are necessary to describe fully the behavior of the common-emitter configuration: one for the output or collector-emitter circuit and the other for the input or base-emitter circuit. Both are shown in Figure 4-7.

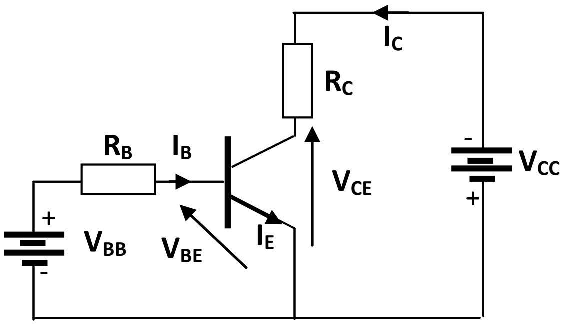


Figure 4-7 : BJT analysis

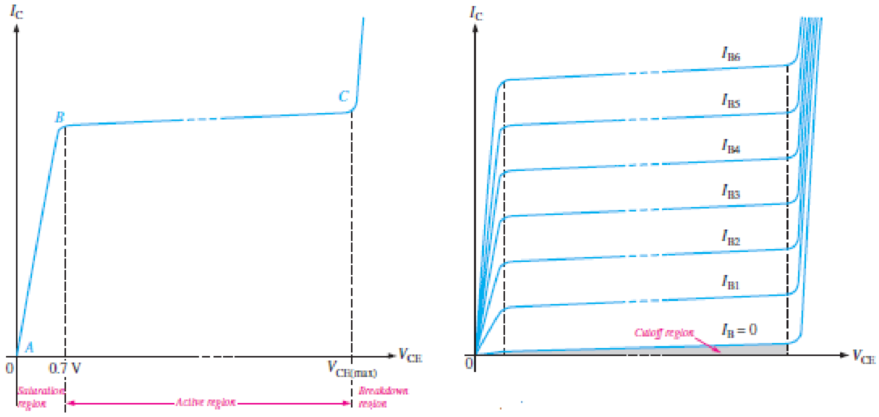


Figure 4-8 : intput and output characteristics of a BJT in common emitter configuration

There are four basic regions as indicated in the Figure 4-8. These regions are :

- **Saturation region**: The region where I_C increases with V_{CE} In this region, both junctions of the transistor are forward biased.
- **Cutoff region**: Located below the I_B=0 line, where both junctions are reverse biased.
- **Active region**: The area between the saturation and cutoff regions, where the curves are nearly parallel to the x-axis.
- **Breakdown region** When V_{CE} (or V_{CB}) becomes very large in reverse bias, the collector–base junction undergoes breakdown. In this region, a sharp increase in collector current occurs, even with little or no base current. Operation in this region is normally avoided, as it may damage the transistor unless designed for avalanche operation.

A- DC Load Line

This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y-axis to the cutoff value where V_{CE}=V_{CC} on the x-axis, as shown in

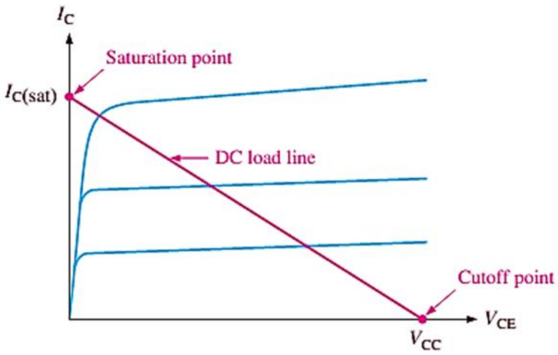


Figure 4-9 : DC Load Line

Two point

- The first point: when the collector current I_C=0, then collector-emitter voltage is maximum and is equal to V_{CC}.

$$V_{CC} = V_{CE} \tag{4.5}$$

- The second point: when the collector emitter voltage V_{CE}=0; the collector current is maximum and is equal

$$I_C = \frac{V_{CE}}{R_C} \tag{4.6}$$

B- **The Operating Point**

The term Basing, refers broadly to the application of DC voltages to establish specific current and voltage levels in a circuit. In transistor amplifiers, this DC bias sets an operating point on the device's characteristic curves, defining the region used for signal amplification. Since this point remains fixed under no-signal conditions, it is referred to as the quiescent point (or Q-point). The word "quiescent" implies a state of rest or inactivity. Figure 4-10 illustrates a typical output characteristic with four possible operating points marked.

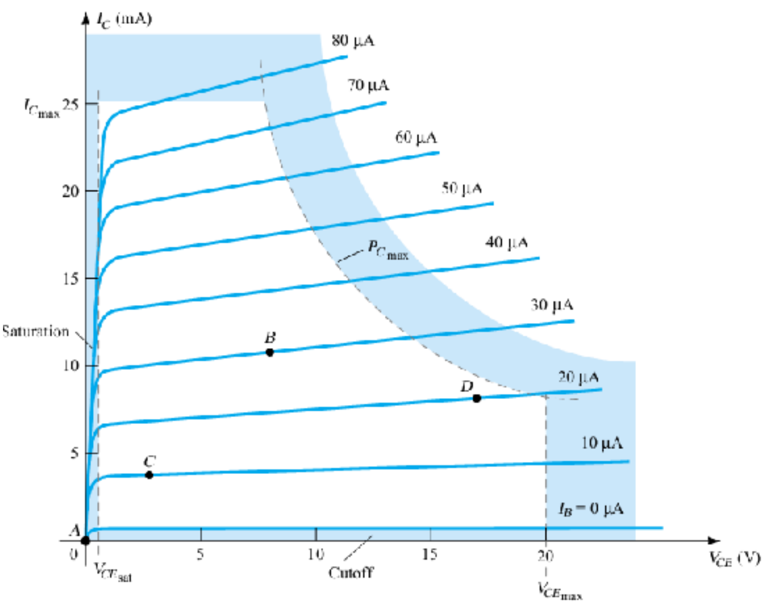


Figure 4-10 : The Operating Point

- At A no bias
- At B suitable bias for signal amplification
- At C close to the saturation and Cut off region
- At D close to the maximum voltage and power level.

4.5.2 Importance of Biasing

Biasing sets the DC operating point (Q-point) needed for an amplifier to work linearly. Without the correct DC voltages at the input and output, the amplifier may enter saturation or cutoff when a signal is applied.

Figure 4-11 illustrates the results of proper and improper DC biasing in an inverting amplifier:

- In part (a), the output is an amplified but inverted version of the input, shifted by 180°. The output swings symmetrically above and below the DC bias level, **VDC (out)**.
- In part (b), the positive half of the output is clipped because the Q-point is set too close to cutoff.
- In part (c), the negative half of the output is clipped because the Q-point is too close to saturation

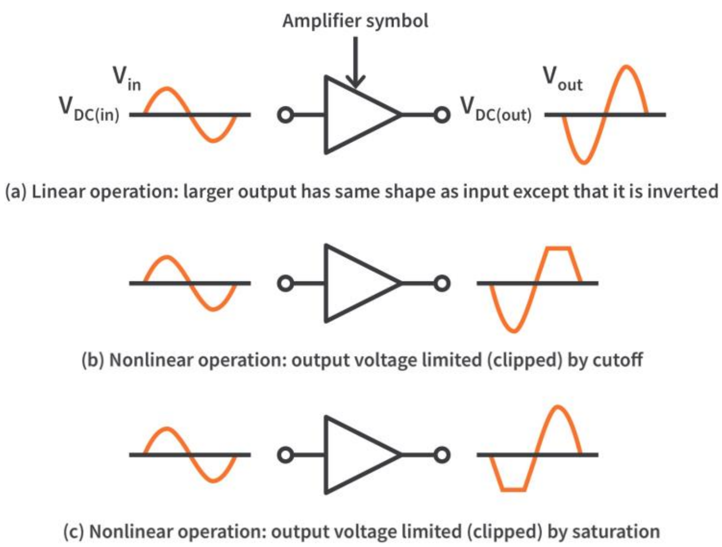


Figure 4-11 : Examples of linear and nonlinear operation of an inverting amplifier (the traingle symbol)

4.5.2.1 BJT Biasing Circuits

a-Base Bias

This circuit is also called the **Fixed Bias Circuit.**The two resistors, $\mathbf{R_B}$ and $\mathbf{R_C}$, are used to provide the required biasing voltages.

By applying Kirchhoff's Voltage Law (KVL) to the input circuit (**BE Loop**), we obtain the voltage difference across it

$$V_{CC} = R_B I_B + V_{BE} \tag{4.7}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.8}$$

By applying Kirchhoff's Law to the output circuit (**CE Loop**), we obtain

$$V_{CC} = R_C I_C + V_{CE} \tag{4.9}$$

$$V_{CE} = V_{CE} - R_C I_C \tag{4.10}$$

We deduce the definition of the current gain in the common-emitter configuration

$$I_C = \beta I_B \tag{4.11}$$

$$I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \tag{4.12}$$

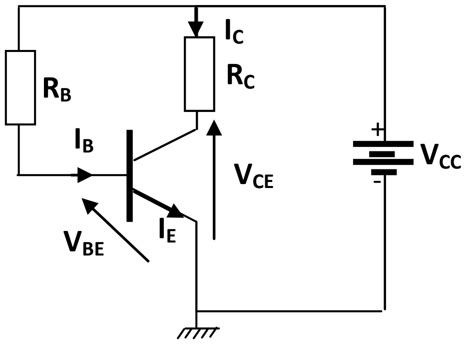


Figure 4-12 : Base Bias

Load line analysis

To simplify Apply Kirchhoff's Law to the output loop of the transistor circuit: We obtain

$$V_{CE} = V_{CE} - R_C I_C \tag{4.13}$$

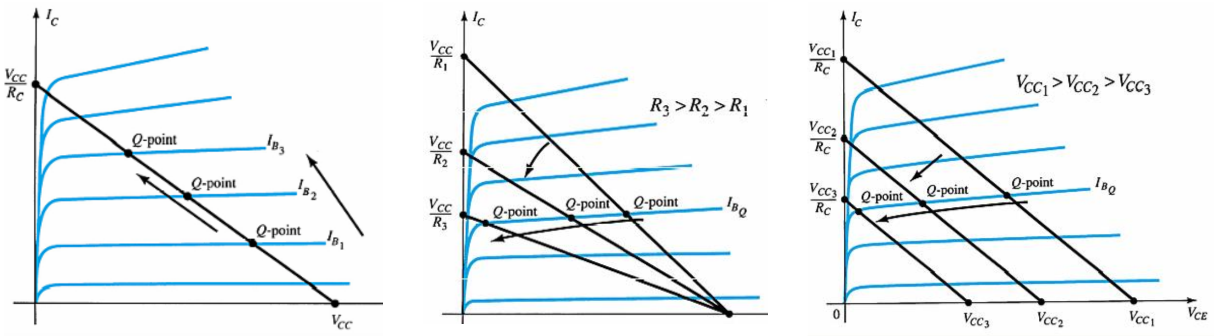
- $I_{C(sat)}$ occurs when transistor operating in saturation region

$$I_{Csat} = \left. \frac{V_{CC}}{R_C} \right|_{V_{CE}=0} \tag{4.14}$$

- $V_{CE(off)}$ occurs when transistor operating in cut-off region

$$V_{CEoff} = V_{CC} = V_{Ce}\big|_{I_C=0} \tag{4.15}$$

The resulting load line for Fixed Bias configuration design is shown in figure 4-13. If the base current I_B is varied by adjusing the base resistor R_B , the Q -point moves up or down the load line as illustrated in Figure 4-13.a for increasing values of I_B . When the supply voltage V_{CC} remains constant and the collector resistor R_C increased, the load line will shift as shown in Figure 4-13.b If I_B is held fixed, the Q -point will move as shown in the same figure. If R_C is fixed and V_{CC} reduced, the load line shifts as shown in Figure 4-13.c



a) varying I_B b) Increasing Rc c) decreasing Vcc

Figure 4-13 : : Circuit Values Affect the Q-Point

b-Emitter-Feedback Bias:

It contains an emitter resistor to improve the stability level over fixed bias.

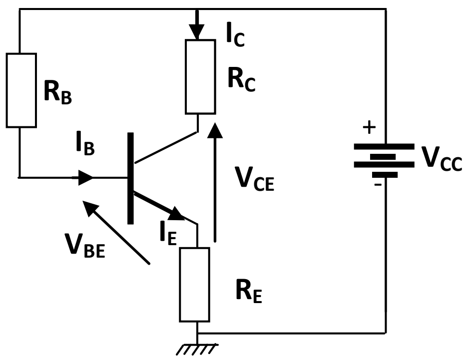


Figure 4-14 : Emitter-Feedback Bias

Base Emitter Loop: Applying KVL wehave

$$V_{CC} = R_B I_B + V_{BE} + R_E I_E \tag{4.16}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} \tag{4.17}$$

Collector Emitter Loop:

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E \tag{4.18}$$

Assume;

$$I_C \approx I_E \tag{4.19}$$

$$V_{CC} = (R_C + R_E) I_C + V_{CE} \tag{4.20}$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_C \tag{4.21}$$

The magnitude of the collector current

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E} \tag{4.22}$$

Lode Line analysis for the emitter bias configuration

To simplify Apply Kirchhoff's Law to the output loop of the transistor circuit: We obtain

$$V_{CE} = V_{CE} - (R_C + R_E) I_C \tag{4.23}$$

- $I_{C(sat)}$ occurs when transistor operating in saturation region

$$I_{Csat} = \left. \frac{V_{CC}}{R_C + R_E} \right|_{V_{CE}=0} \tag{4.24}$$

- $V_{CE(off)}$ occurs when transistor operating in cut-off region

$$V_{CEoff} = V_{CC} = V_{Ce} \big|_{I_C=0} \tag{4.25}$$

The resulting load line for the emitter bias design is shown in figure 1-15.

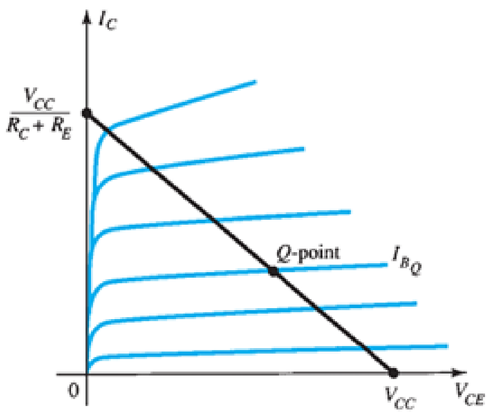


Figure 4-15 : Emitter bias load line

- **Improved Bias Stability**

Adding an emitter resistor to the BJT's DC bias circuit improves stability by helping the bias currents and voltages remain near their original set points, even when external conditions like temperature or transistor beta vary.

.

Without R_E	With R_E
$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$	$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}\right)$

f- Collector feedback Bias

In Figure 4-16, the base resistor R_B is connected to the collector instead of V_{CC}. The collector voltage is therefore used to bias the base-emitter junction. The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable. When I_C tries to increase, it drops more voltage across R_C, thereby causing V_C to decrease. When V_C decreases, there is a decrease in voltage cross R_B, which decreases I_B. The decrease in I_B produces less I_C which drops less voltage across R_C and thus offsets the decrease in V_C.

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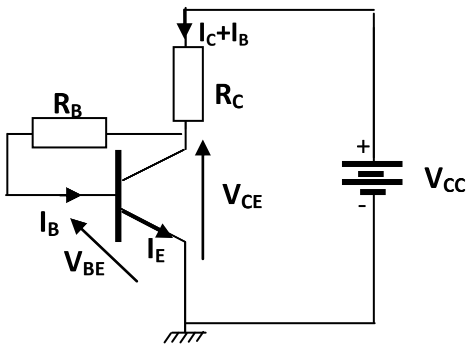


Figure 4-16 : Collector feedback Bias

Applying KVL:

$$V_{CC} = R_C(I_C + I_B) + V_{BE} + R_B I_B \tag{4.26}$$

$$V_{CC} = R_C \beta_{DC} I_B + R_C I_B + V_{BE} + R_B I_B \tag{4.27}$$

$$V_{CC} = (\beta_{DC} + 1)R_C I_B + V_{BE} + R_B I_B \tag{4.28}$$

$$I_B = \frac{V_{CC} - V_{BE}}{(\beta_{DC} + 1)R_C + R_B} \tag{4.29}$$

The magnitude of the collector current

$$I_C = \beta_{DC} \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta_{DC}) R_C} \tag{4.30}$$

The **load line equation** for the self-bias circuit, based on Kirchhoff's Voltage Law (KVL) around the **collector loop**, is written as:

$$V_{CC} = R_C I_E + V_{CE} \tag{4.31}$$

$$V_{CC} = R_C (I_C + I_B) + V_{CE} \tag{4.32}$$

$$V_{CC} = R_C \left(I_C + \frac{I_C}{\beta_{DC}} \right) + V_{CE} \tag{4.33}$$

$$V_{CC} = R_C I_C + R_C \frac{I_C}{\beta_{DC}} + V_{CE} \tag{4.34}$$

$$V_{CC} = I_C \left(1 + \frac{R_C}{\beta_{DC}} \right) + V_{CE} \tag{4.35}$$

$$I_C = \frac{V_{CC} - V_{CE}}{1 + \frac{R_C}{\beta_{DC}}} \tag{4.36}$$

- $I_{C(sat)}$ occurs when transistor operating in saturation region

$$I_{Csat} = \left. \frac{V_{CC}}{1 + \frac{R_C}{\beta_{DC}}} \right|_{V_{CE}=0} \tag{4.37}$$

- $V_{CE(off)}$ occurs when transistor operating in cut-off region

$$V_{CEoff} = V_{CC} = V_{Ce}\big|_{I_C=0} \tag{4.38}$$

g- Voltage divider bias

Figure 4-17 shows the most widely used biasing circuit. Notice that the base circuit contains a voltage divider (R_1 and R_2). Because of this, the circuit is called **voltage-divider bias (VDB).**

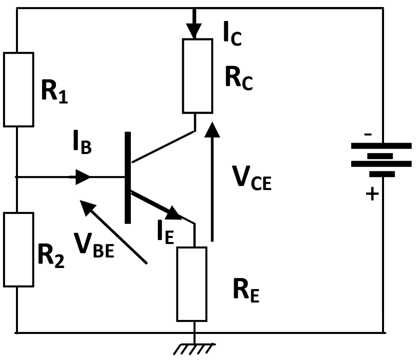


Figure 4-17 : Voltage Divider Bias

✓ **Exact analysis**

The input section of the network in Figure 4-17 can be redrawn as shown in Figure 4-18 for DC analysis. Apply Thevenin's theorem to the portion of the circuit to the left of point B, replacing V_{CC} with a short to ground and disconnecting the transistor.

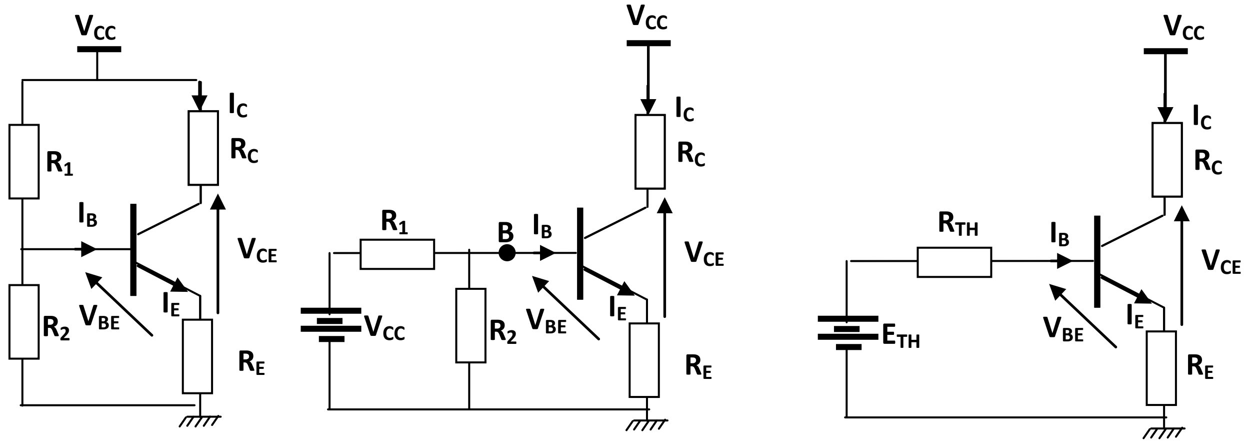


Figure 4-18 : Thevenizing the bias circuit

The voltage at point B with respect to ground is :

$$E_{TH} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{4.39}$$

$$R_{TH} = \frac{R_1 \times R_2}{R_1 + R_2} \tag{4.40}$$

Applying KVL

$$E_{TH} = R_{TH} I_B + V_{BE} + R_E I_E \tag{4.41}$$

Substituting $I_E=(1+\beta)\ I_B$ and solving for I_B yields

$$E_{TH} = R_{TH} I_B + V_{BE} + R_E (1+\beta)\ I_B \tag{4.42}$$

$$I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + R_E(1+\beta)} \tag{4.43}$$

The magnitude of the I_C

$$I_C = \beta \left(\frac{E_{TH} - V_{BE}}{R_{TH} + R_E(1+\beta)} \right) \tag{4.44}$$

Lode Line analysis for the Voltage Divider Bias

To simplify Apply Kirchhoff's Law to the output loop of the transistor circuit: We obtain :

$$V_{CC} = V_{CE} + R_E I_E + R_C I_C \tag{4.45}$$

$$V_{CC} = V_{CE} + R_E (I_C + I_B) + R_C I_C \tag{4.46}$$

Let's assume that Also, $(I_C \succ\succ I_B)$

$$V_{CC} = V_{CE} + (R_C + R_E) I_C \tag{4.47}$$

$$I_C = \frac{V_{CE} - V_{CC}}{R_C + R_E} \tag{4.48}$$

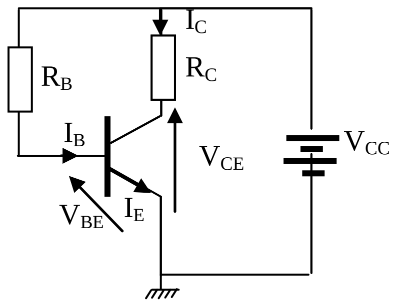
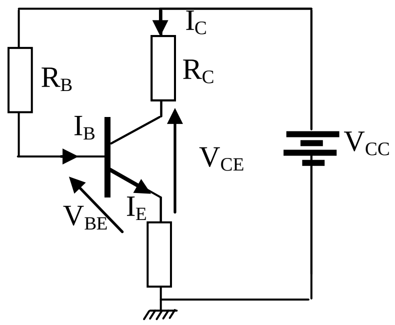
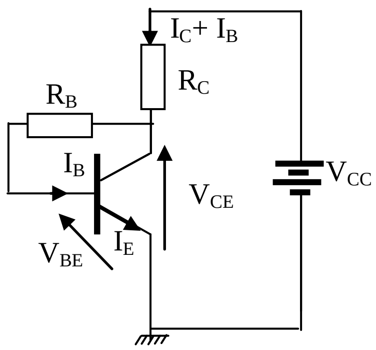
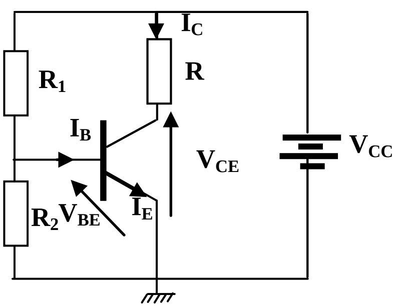
- $I_{C(sat)}$ occurs when transistor operating in saturation region

$$I_{Csat} = \left. \frac{V_{CC}}{R_C + R_E} \right|_{V_{CE}=0} \tag{4.49}$$

- $V_{CE(off)}$ occurs when transistor operating in cut-off region

$$V_{CEoff} = V_{CC} = \left. V_{Ce} \right|_{I_C=0} \tag{4.50}$$

Table 4-2 : Symmary of transistor biasing Circuits

 **Base Bias**	$I_B = \frac{V_{CC} - V_{BE}}{R_B}$
	$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$
	$V_{CE} = V_{CE} - R_C I_C$
	$(V_{CC}, 0), \left(0, \frac{V_{CC}}{R_C}\right)$
 **Emitter bias**	$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$
	$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}\right)$
	$V_{CE} = V_{CE} - (R_C + R_E)I_C$
	$(V_{CC}, 0), \left(0, \frac{V_{CC}}{R_C + R_E}\right)$
 **Collector feedback Bias**	$I_B = \frac{V_{CC} - V_{BE}}{(\beta_{DC} + 1)R_C + R_B}$
	$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{(\beta_{DC} + 1)R_C + R_B}\right)$
	$V_{CE} = V_{CC-} I_C \left(1 + \frac{R_C}{\beta_{DC}}\right)$
	$(V_{CC}, 0), \left(0, \frac{V_{CC}}{1 + \frac{R_C}{\beta_{DC}}}\right)$
 **Voltage Divider Bias**	$I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + R_E(1+\beta)}$
	$I_C = \beta\left(\frac{E_{TH} - V_{BE}}{R_{TH} + R_E(1+\beta)}\right)$
	$V_{CE} = V_{CC} - (R_C + R_E)I_C$
	$(V_{CC}, 0), \left(0, \frac{V_{CC}}{R_C + R_E}\right)$

4.6 BJT Amplifier

A BJT amplifier is a circuit that amplifies small input signals by controlling a larger output current in response to the input. BJT amplifiers are classified based on their configuration: **Common Emitter (CE)**, **Common Base (CB),** and **Common Collector (CC)**. Each configuration has unique characteristics suited for different applications.

4.6.1 BJT AC equivalent circuit

We now start our investigation of the Bipolar Junction Transistor's (BJT) AC response by looking at the models that are most frequently used to depict the transistor in the sinusoidal AC domain. The input signal's amplitude is a key factor in the AC analysis of transistor circuits. Whether to use small-signal or large-signal analysis approaches depends on the signal's amplitude.

There are three modules commonly used in the small-signal AC analysis of transistor networks 1- The Re model 2- The hybrid π model 3- The hybrid equivalent model

4.6.2 Small signal analysis of BJT

The importance parameters for Two-Port system

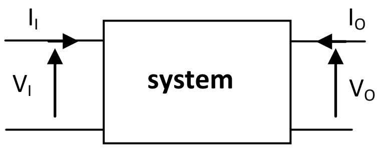


Figure 4-19 : Defining the Important Parameters of Any System

Table 4-3 : The importance parameters for Two-Port system

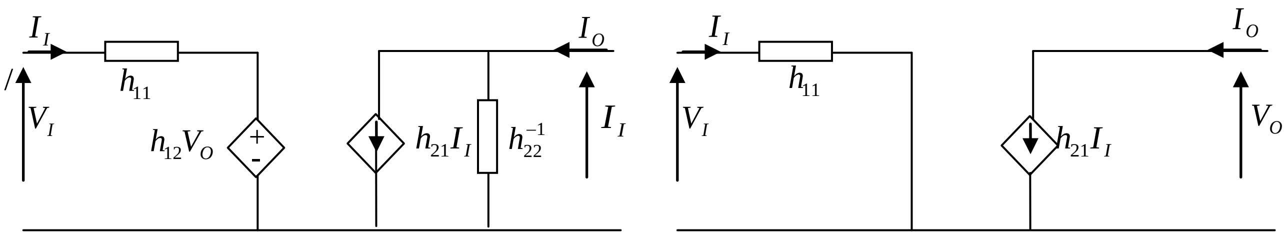
Voltage Gain	$G_V = \frac{V_O}{V_I}$
Current Gain	$G_I = \frac{I_O}{I_I}$
Power Gain	$G_p = G_V \times G_I$
Input impedance	$Z_I = \frac{V_I}{I_I}$
Ouput impedance	$Z_O = \frac{V_O}{I_O}$

4.6.3 Equivalent Model of transistor

4.6.3.1 Hybrid Equivalent Model

The hybrid parameters: h_{11}, h_{12}, h_{21} and h_{22} are developed and used to model the transistor. These parameters can be found in a specification sheet for a transistor (see Table 2-3)

The complete ac equivalent circuit for the basic three-terminal linear device is indicated in Figure 4-20.a, with a new set of subscripts for the h-parameters. This circuit, can be further simplified if a value for the parameter $1/h_{22}$ is not provided. In that case, we can safely assume that $h_{12}=0$ or $1/h_{22}=\infty$ resulting in the approximate hybrid equivalent circuit shown Figure 4-20.b.



(a) Generalized H-parameter model for a BJT (b) Simplified H-parameter model for a BJT

Figure 4-20 : H-parameter transistor model.

2

4.6.4 The common- Emitter Amplifier

4.6.4.1 Common-emitter voltage-divider bias configuration

Figure 4-21 illustrates a **common-emitter amplifier** using a voltage-divider bias. It includes coupling capacitors, C_1 at the input and C_3 at the output, as well as a bypass capacitor, C_2, connected from the emitter to ground. The input signal V_i is applied to the base through capacitor C_1, while the output signal Vo is taken from the collector and delivered to the load through capacitor C_3.

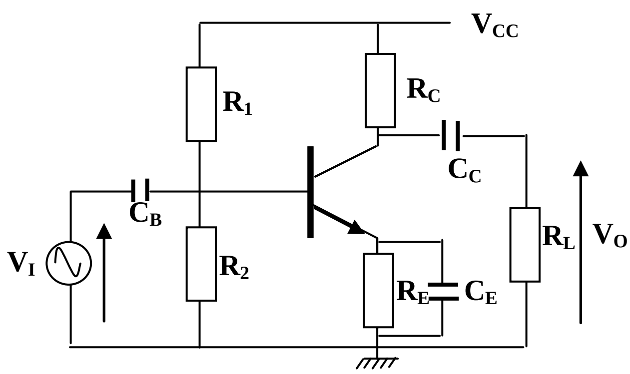


Figure 4-21 : Common-emitter voltage-divider bias configuration

✓ **Coupling Capacitor and Bypass Capacitor**

➢ **Coupling Capacitor**

- Used to transfer AC signals between two stages of a circuit while blocking DC components.
- Ensures that the DC biasing of the two stages does not interfere with each other.

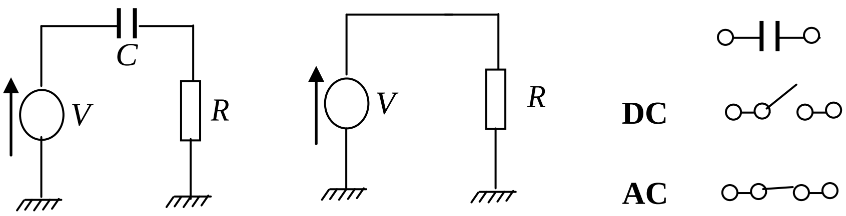


Figure 4-22 : Coupling Capacitor

➢ **Bypass capacitor**

A **bypass capacitor** is similar to a coupling capacitor because it appears open to direct current and shorted to alternating current. But it is not used to couple a signal between two points. Instead, it is used to create an ac ground.

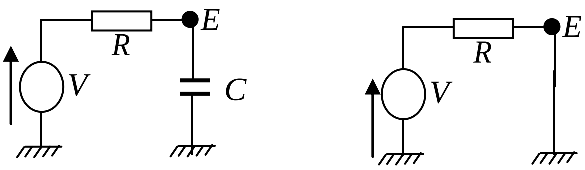


Figure 4-23 : Bypass capacitor

- **AC equivalent circuit for the amplifier**

For AC analysis we need

- AC equivalent circuit
- Replace the transistor with the equivalent model to find out the AC response
- **Step 1:** short circuit all the dc sources
- **Step 2:** short all the capacitors
- **Step 3**: redraw the network removing all the elements which are short circuited in Step 1 and Step 2

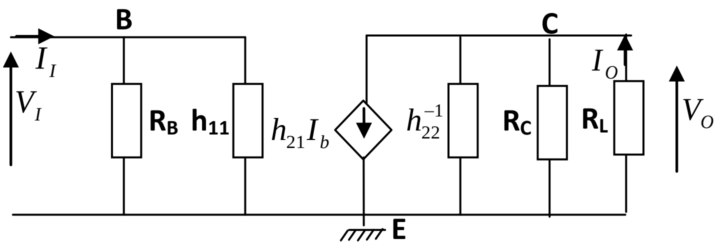


Figure 4-24 : AC-equivalent circuit (Common-emitter amplifier)

Voltage gain $G_V = \dfrac{V_O}{V_I}$

$$V_O = -\left(h_{22}^{-1} // R_C // R_L\right) h_{21} I_B \tag{4.51}$$

$$V_I = h_{11} I_B \tag{4.52}$$

$$G_V = -\frac{\left(h_{22}^{-1} // R_C // R_L\right) h_{21} I_B}{h_{11} I_B} \tag{4.53}$$

$$G_V = -\frac{\left(h_{22}^{-1} // R_C // R_L\right) h_{21}}{h_{11}} \tag{4.54}$$

Input Impedance $Z_I = \dfrac{V_I}{I_I}$

$$V_I = \left(\frac{h_{11} \times R_B}{h_{11} + R_B}\right) I_I \tag{4.55}$$

$$Z_I = \frac{h_{11} \times R_B}{h_{11} + R_B} \tag{4.56}$$

$$Z_I = h_{11} \tag{4.57}$$

$$RB \geq 10 h_{11} \tag{4.58}$$

Current gain $G_I = \dfrac{I_O}{I_I}$

$$\left.\begin{array}{l} V_O = -R_L I_O \\ V_I = Z_I I_I \end{array}\right\} \Rightarrow \frac{I_O}{I_I} = -\frac{V_O}{R_L}\frac{Z_I}{V_I} = -G_V \frac{Z_I}{R_L} \tag{4.59}$$

Ouput Impedance $Z_O = \dfrac{V_O}{I_O}$

We use Thévenin's theorem:

• Disconnect the load

• Short-circuit the generator at the input V_I=0

• Apply a voltage Vo at the output, which injects a current I_O

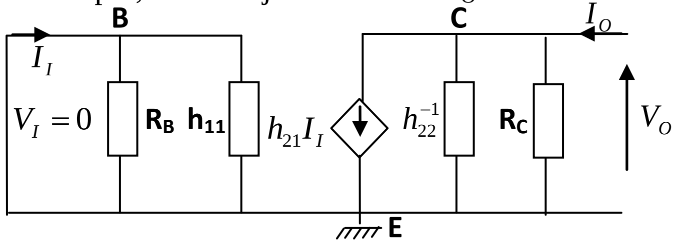


Figure 4-25 : Determination of ouput Impedance (Common-emitter amplifier)

$$V_O = -\left(h_{22}^{-1} // R_C\right)\left(I_O - h_{21} I_B\right) \tag{4.60}$$

$$V_I = h_{11} I_B = 0 \Rightarrow I_B = 0 \tag{4.61}$$

$$V_O = \left(h_{22}^{-1} // R_C\right) I_O \tag{4.62}$$

$$Z_O = \frac{\left(h_{22}^{-1} // R_C\right) I_O}{I_O} = h_{22}^{-1} // R_C \tag{4.63}$$

$$Z_O = R_C \tag{4.64}$$

$$R_C \geq 10 h_{22}^{-1} \tag{4.65}$$

- **Phase Relationship**

The negative sign indicates that 180° phase shift occurs between the input and output signals.

4.6.4.2 A common-emitter amplifier Unbypassed voltage-divider bias configuration

We consider the same circuit as in the previous section, except that the bypass capacitor **CE** has been removed. The modified circuit is illustrated in the figure below.

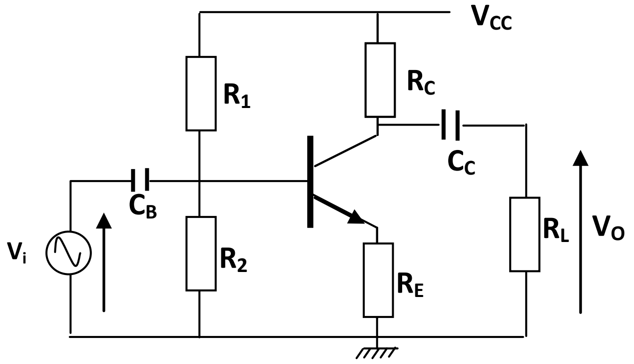


Figure 4-26 : A common-emitter amplifier Unbypassed voltage-divider bias configuration

Fiure 4-27 shown the equivalent circuit for the A common-emitter amplifier unbypassed voltage-divider bias configuration

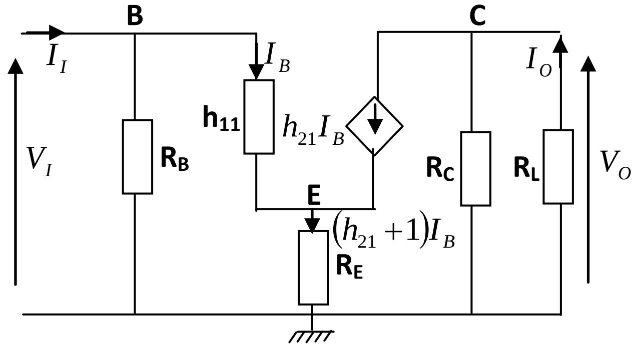


Figure 4-27 : AC-equivalent circuit for the a CE amplifier unbypassed

Voltage gain $G_V = \frac{V_O}{V_I}$

$$V_O = -(R_C // R_L) h_{21} I_B \tag{4.66}$$

$$V_I = [h_{11} + R_E I(h_{21} + 1)] I_B \tag{4.67}$$

$$G_V = -\frac{(R_C // R_L) h_{21} I_B}{V_I = [h_{11} + R_E I(h_{21} + 1)] I_B} \tag{4.68}$$

$$G_V = -\frac{(R_C // R_L) h_{21}}{h_{11} + R_E I(h_{21} + 1)} \tag{4.69}$$

Input Impedance $Z_I = \frac{V_I}{I_I}$

$$V_I = R_B (I_I - I_B) \tag{4.70}$$

$$V_I = (h_{11} + R_E (h_{21} + 1)) I_B \tag{4.71}$$

$$V_I = R_B \left(i_e - \frac{V_e}{(h_{11} + R_E (h_{21} + 1))} \right) \tag{4.72}$$

$$V_I [h_{11} + R_E (h_{21} + 1) + R_B] = I_I [(h_{11} + R_{E2} (h_{21} + 1)) R_B] \tag{4.73}$$

$$Z_I = \frac{V_I}{I_I} = \frac{(h_{11} + R_E (h_{21} + 1)) \times R_B}{h_{11} + R_E (h_{21} + 1) + R_B} \tag{4.74}$$

4.6.4.3 Common Collector Amplifier (emitter follower)

An emitter-follower circuit using voltage-divider bias is illustrated in Figure 4-28. The input signal is coupled to the base through a capacitor, while the output signal is taken from the emitter through another capacitor. The collector is maintained at ac ground. This configuration does not produce phase inversion, and the output amplitude is nearly equal to that of the input.

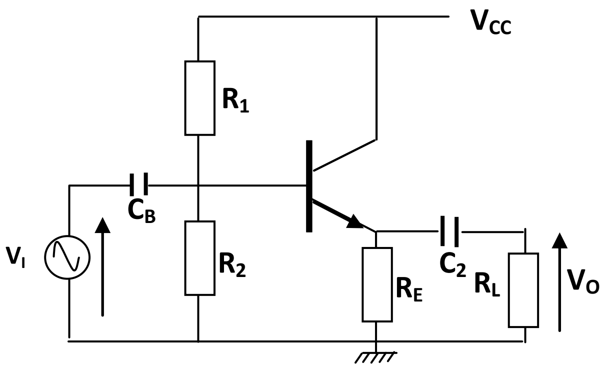


Figure 4-28 : Common collectoramplifier (emmitter follower)

Figure 4-29 shown the equivalent circuit for the common collector amplifier (emitter follower)

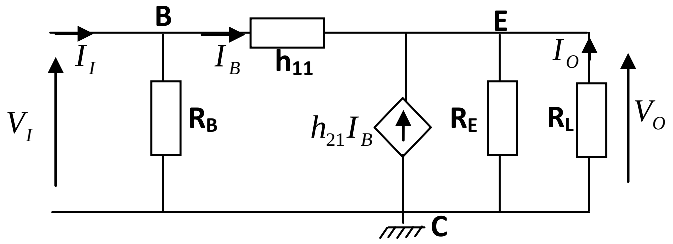


Figure 4-29 : Hybrid Equivalent for the common collector amplifier (emitter follower)

- **Voltage gain** $G_V = \dfrac{V_O}{V_I}$

$$V_O = (R_E // R_L)(h_{21}+1)I_B \quad (4.75)$$

$$V_I = h_{11}I_B + V_O \quad (4.76)$$

$$V_I = [h_{11} + (R_E // R_L)(h_{21}+1)]I_B \quad (4.77)$$

$$G_V = \frac{(R_E // R_L)(h_{21}+1)I_B}{[h_{11} + (R_E // R_L)(h_{21}+1)]I_B} \quad (4.78)$$

$$G_V = \frac{(R_E // R_L)(h_{21}+1)}{[h_{11} + (R_E // R_L)(h_{21}+1)]} \approx 1 \quad (4.79)$$

Phase Relationship

Emitter-follower (common-collector) conguration has no phase shift between input and output

Input Impedance $Z_I = \dfrac{V_I}{I_I}$

$$V_I = R_B(I_I - I_B) \quad (4.80)$$

$$V_I = (h_{11} + (h_{21}+1)(R_E // R_L))I_B \quad (4.81)$$

$$I_B = \frac{V_I}{h_{11} + (h_{21}+1)(R_E // R_L)} \quad (4.82)$$

$$V_I = R_B\left(I_I - \frac{V_I}{h_{11} + (h_{21}+1)(R_E // R_L)}\right) \quad (4.83)$$

$$V_I[h_{11} + (h_{21}+1)(R_E // R_L) + RB] = I_I[(h_{11} + (h_{21}+1)(R_E // R_L))RB] \quad (4.84)$$

$$Z_I = \frac{V_I}{I_I} = \frac{(h_{11} + (h_{21}+1)(R_E // R_L))RB}{h_{11} + (h_{21}+1)(R_E // R_L) + RB} \quad (4.85)$$

Ouput Impedance $Z_O = \frac{V_O}{I_O}$

We use Thévenin's theorem:

- Disconnect the load
- Short-circuit the generator at the input $V_I=0$
- Apply a voltage Vo at the output, which injects a current I_O

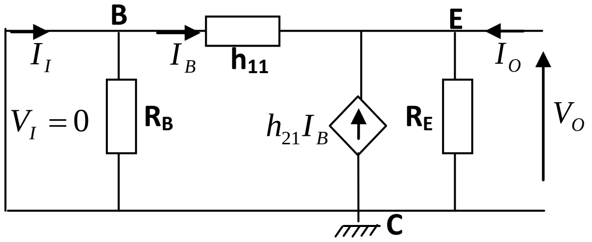


Figure 4-30 : Output impedance C-C Configuration

$$V_O = R_E\left(I_O + (h_{21}+1)I_B\right) \tag{4.86}$$

$$V_O = 0 \Rightarrow h_{11}I_B + V_O \Rightarrow I_B = -\frac{V_O}{h_{11}} \tag{4.87}$$

$$V_O = R_E\left(I_O - (h_{21}+1)\frac{V_O}{h_{11}}\right) \Rightarrow V_O(1+(h_{21}+1)\frac{R_E}{h_{11}}) = R_E\, I_O \tag{4.88}$$

$$Z_O = \frac{V_O}{I_O} = \frac{R_E h_{11}}{h_{11} + (h_{21}+1)R_E} \tag{4.89}$$

$$h_{21} \succ\succ 1, \quad R_E h_{21} \succ\succ h_{11} \quad Z_O = \frac{V_O}{I_O} = \frac{h_{11}}{h_{21}} \tag{4.90}$$

4.6.4.4 Common Base Amplifier

A common-base amplifier, as shown in Figure 4-31, uses the base as the common terminal, which is held at AC ground by capacitor C_2. The input signal is applied to the emitter through a coupling capacitor, and the output is taken from the collector, also coupled through a capacitor to the load resistor.

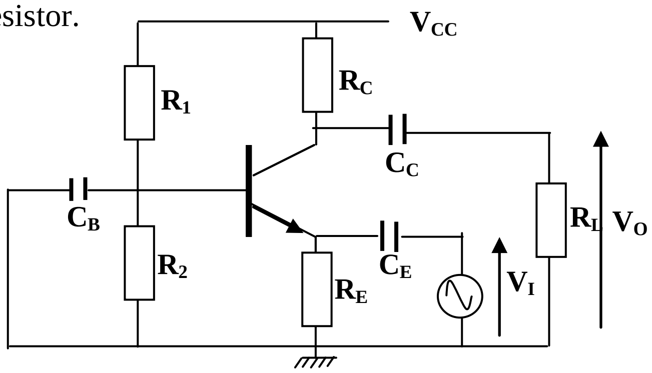


Figure 4-31 : Common-base amplifier

Figure 4-32 shown AC the equivalent circuit for Common-base amplifier

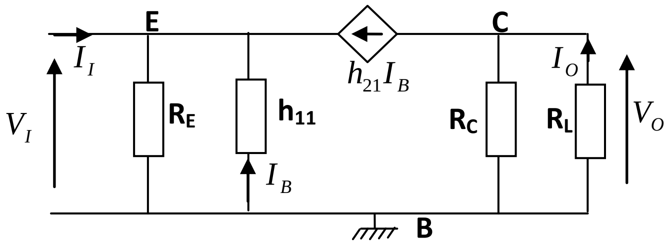


Figure 4-32 : AC the equivalent circuit of the Common-base amplifier

Voltage gain $G_V = \frac{V_O}{V_I}$

$$V_O = -(R_C // R_L)h_{21}I_B \qquad (4.91)$$

$$V_I = -h_{11}I_B \qquad (4.92)$$

$$G_V = \frac{V_O}{I_O} = \frac{(R_C // R_L)h_{21}}{h_{11}} \qquad (4.93)$$

Phase Relationship

The Common Base Amplifier has no phase shift between input and output

Input Impedance $Z_I = \frac{V_I}{I_I}$

$$V_I = (R_E // h_{11}))(I_I + h_{21}I_B) \qquad (4.94)$$

$$V_I = -h_{11}I_B \Rightarrow I_B = -\frac{V_O}{h_{11}} \qquad (4.95)$$

$$V_I = (R_E // h_{11}))\left(I_I - \frac{h_{21}}{h_{11}}V_0\right) \qquad (4.96)$$

$$V_I\left(1 + \frac{(R_E // h_{11})h_{21}}{h_{11}}\right) = (R_E // h_{11})I_I \qquad (4.97)$$

$$Z_I = \frac{V_I}{I_I} = \frac{(R_E // h_{11})h_{11}}{h_{11} + (R_E // h_{11})h_{21}} \qquad (4.98)$$

$$(R_E // h_{11})h_{21} \succ\succ h_{11} \Rightarrow Z_I = \frac{h_{11}}{h_{21}} \qquad (4.99)$$

Ouput Impedance $Z_O = \frac{V_O}{I_O}$

We use Thévenin's theorem:

- Disconnect the load
- Short-circuit the generator at the input V_I=0
- Apply a voltage Vs at the output, which injects a current I_O

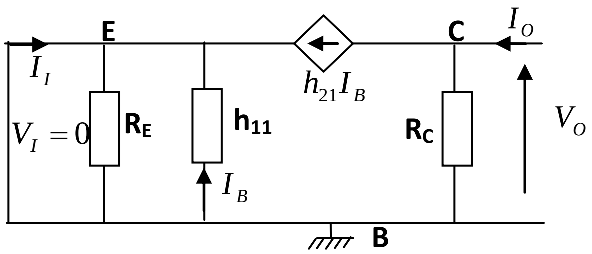


Figure 4-33 : Output impedance C-B configuration

$$V_O = R_C(I_O - h_{21}I_B) \quad (4.100)$$

$$V_I = 0 \Rightarrow -h_{21}I_B = 0 \Rightarrow I_B = 0 \quad (4.101)$$

$$V_O = R_C I_O \Rightarrow Z_I = R_C \quad (4.102)$$

Summary of the tree common transistor amplifier configurations is presented in Table 4.4.

Table 4-4 : Summary of the tree Common Amplifi er Confi gurations

	G_V	Z_I	Z_O	Phase Relationship
Common emitter (CE)	$-\frac{(h_{22}^{-1} // R_C // R_L)h_{21}}{h_{11}}$	h_{11}	R_C	180 degrees
Common base (CB)	$\frac{(R_C // R_L)h_{21}}{h_{11}}$	$\frac{h_{11}}{h_{21}}$	R_C	0 degrees
Common collector (emitter follower) (CC)	≈ 1	$\frac{(h_{11} + (h_{21}+1)(R_E // R_L))RB}{h_{11} + (h_{21}+1)(R_E // R_L) + RB}$	$\frac{h_{11}}{h_{21}}$	0 degrees

4.6.5 Multistage transistor Amplifiers

Two or more amplifiers may be connected in cascade, where the output of one amplifier feeds the input of the next. Each amplifier in this arrangement is referred to as a stage. The primary purpose of a multistage configuration is to increase the total voltage gain. Although discrete multistage amplifiers are less common today than in the past, studying them helps illustrate how circuits influence one another when interconnected. The three couplings generally used are: 1- Direct-Coupled 2- RC coupling 3- Transformer coupling

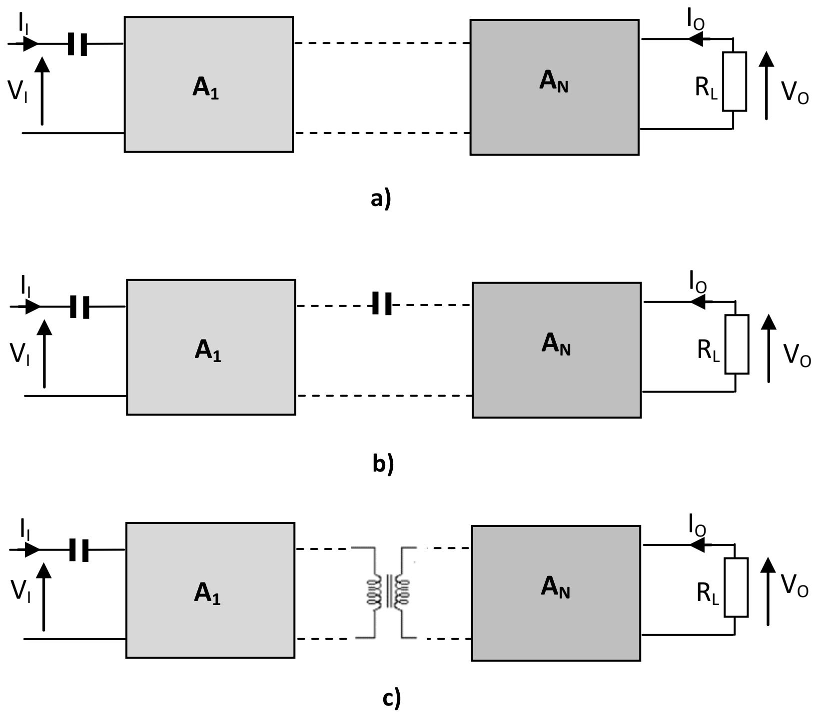


Figure 4-34 : Multistage transistor Amplifiers
a) Direct-Coupled b) RC coupling c)Transformer coupling

4.6.5.1 Multistage Voltage Gain

The overall voltage gain, Av, of cascaded amplifiers, as shown in Figure 4-35, is the product of the individual voltage gains.

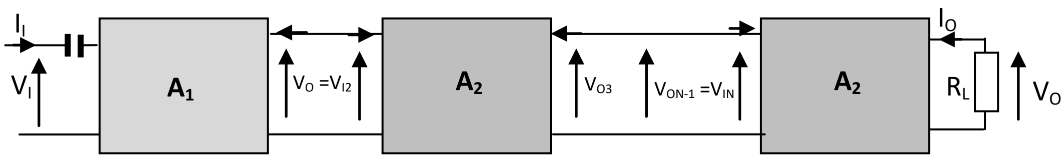


Figure 4-35 : Multistage Voltage Gain

$$G_V = G_{V1} \times G_{V2} \times G_{V3} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots G_{VN} \tag{4.104}$$

Where n is the number of stages.

$$G_{V1} = \frac{V_{O1}}{V_I} \tag{4.105}$$

$$G_{V2} = \frac{V_{O2}}{V_{I2} = V_{O1}} \tag{4.106}$$

$$G_{V3} = \frac{V_{O3}}{V_{I3} = V_{O2}} \tag{4.107}$$

$$G_{VN} = \frac{V_O}{V_{IN} = V_{ON-1}} \tag{4.108}$$

4.7 Darlington Connections

A **Darlington connection** is a connection of two transistors whose overall current gain equals the product of the individual current gains. Since its current gain is much higher, a Darlington connection can have a very high input impedance and can produce very large output currents. Darlington connections are often used with voltage regulators, power amplifiers, and high current switching applications

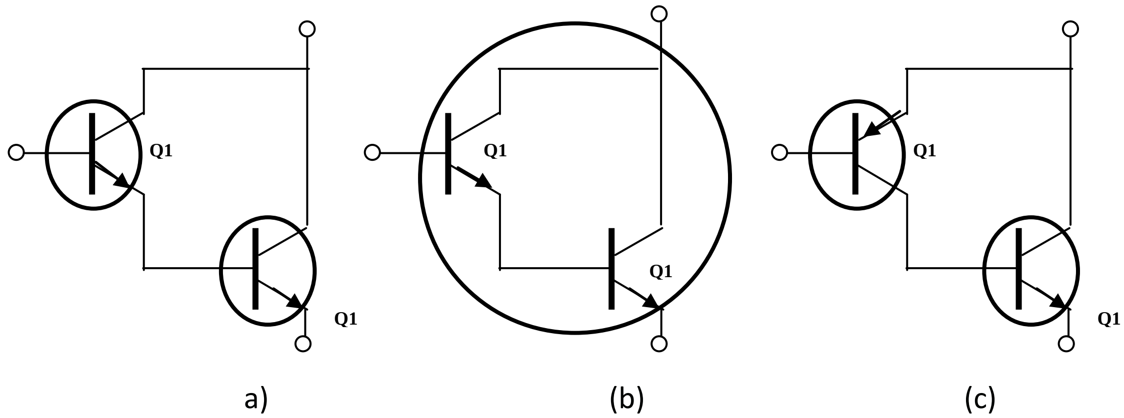


Figure 4-36 : a) Darlington pair; (b) Darlington transistor; (c) complementary Darlington

Figure 4-36a shows a **Darlington pair**. Since the emitter current of Q_1 is the base current for Q_2, the Darlington pair has an overall current gain of:

$$\beta = \beta_1 \beta_2 \tag{4.109}$$

Semiconductor manufacturers can put a Darlington pair inside a single case like that shown in Figure 4-36b. This device, known as a **Darlington transistor**, acts like a single transistor with a very high current gain.

Figure 4-36c shows another Darlington connection called a **complementary Darlington**, a connection of npn and pnp transistors. The collector current of Q_1 is the base current of Q_2. If the pnp transistor has a current gain of β_1 and the npn output transistor has a current gain of β_2 the complementary Darlington acts like a single pnp transistor with a current gain of $\beta_1\beta_2$.

4.8 The BJT as a Switch

In the last part, you saw how a BJT can be used as a **linear amplifier**. The second primary application area is **switching applications**.

4.8.1 Switching Operation

The fundamental functioning of a BJT as a switching device is shown in Figure 4-37

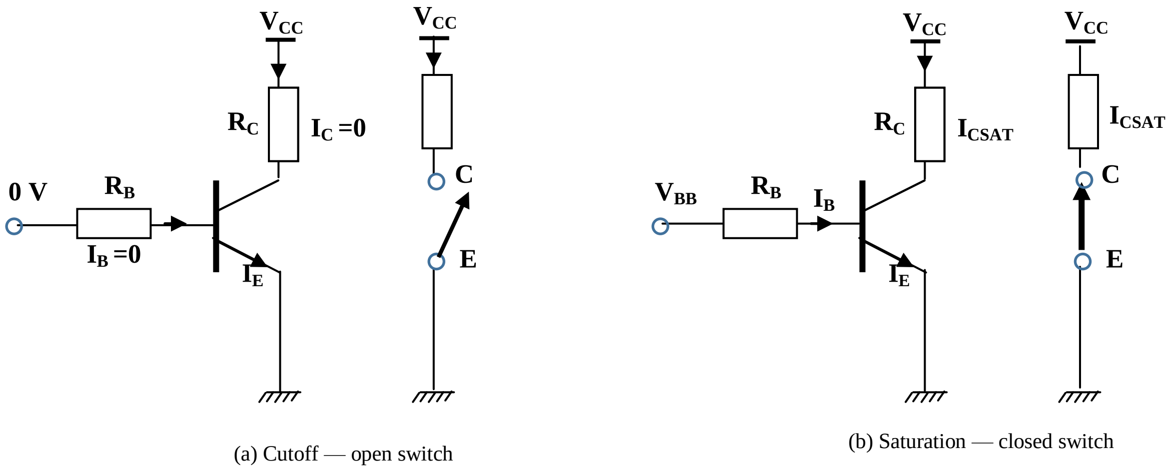


Figure 4-37 : Switching action of an ideal transistor

In part (a), the transistor is in the cutoff region

Cutoff Conditions : As previously stated, when the base-emitter junction is not forward-biased, a transistor is in the cutoff area. All currents are 0 when leakage current is ignored, and V_{CE} and V_{CC} are equal.

$$V_{CE(CUTOFF)} = V_{CC} \qquad (4.110)$$

In part (a), the transistor is in the saturation region

Saturation Conditions As you now know, a transistor is saturated when the base-emitter junction is forward-biased and there is sufficient base current to generate a maximum collector current. The collector saturation current formula is :

$$I_{C(SAT)} = \frac{V_{CC} - V_{CE(SAT)}}{R_C} \tag{4.111}$$

$V_{CE\ (sat)}$ can typically be disregarded because it is much smaller than V_{CC}.

The lowest base current required to achieve saturation is :

$$I_{B(\min)} = \frac{I_{C(SAT)}}{\beta_{DC}} \tag{4.112}$$

To make sure **the transistor is saturated**, I_B should typically be much higher than $I_{B(min)}$.

4.9 Glossary

Francais	Anglaish	العربية
Transistor à jonction bipolaire	Bipolar Junction Transistor	ترانزستور ثنائي القطب
Emitteur	Emitter	الباعث
Collecteur	the collector	الجامع
Base	base	القاعدة
L'émetteur commun	The Common Emitter	الباعث المشترك
La base commune	The Common base	القاعدة المشتركة
collecteur commun (émetteur suiveur)	common collector (emitter follower)	جامع مشترك (متابع الباعث)
Polarisation par résistance de base	Fixed-bias Configuration	الانحياز الثابت (انحياز القاعدة)
Polarisation par réaction d'émetteur	Emitter-Feedback Bias	انحياز الباعث
Polarisation par retour du collecteur Auto-polarisation	Collector-Feedback Bias (self-bias)	دائرة الانحياز الذاتي انحياز التغذية الخلفية
Polarisation par pont de résistances de base	Voltage-Divider Bias	دائرة انحياز مقسم الجهد
La droite de charge	The Load-Line	خط الحمل
Point de repos (point Q)	quiescent point (Q-point)	نقطة السكون (نقطة)

BIPOLAR JUNCTION TRANSISTOR (BJT) Exercises

Exercise 04.1 : Emitter Bias

Calculate the Q-point values (I_{CQ} and V_{CEQ}) for the circuit in Figure 4-38

-

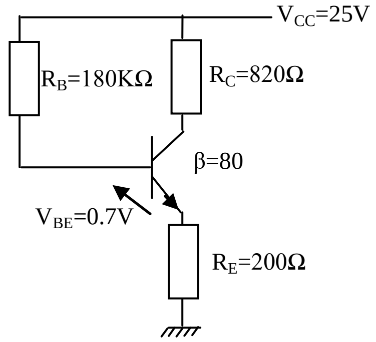


Figure 4-38 : Circuit for Exercise 04.1

Exercise 04.2 : Collector Bias

Calculate the Q-point values (I_{CQ} and V_{CEQ}) for the circuit in Figure 4-39

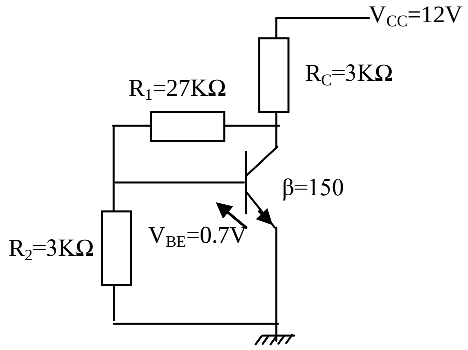


Figure 4-39 : Circuit for Exercise 04.2

Exercise 04.3: Voltage-divider configuratin

Determine the dc bias voltage V_{CEQ} and the current I_{CQ} for Voltage-divider configuratin

for:

$\beta = 100 \quad and \quad \beta = 50$

Withm:

$R_1 = 39K\Omega; R_2 = 9{,}3K\Omega; \; R_C = 100K\Omega; \; R_E = 1{,}5K\Omega$

$V_{CC} = 22 \quad and \; VBE = 0{,}7V$

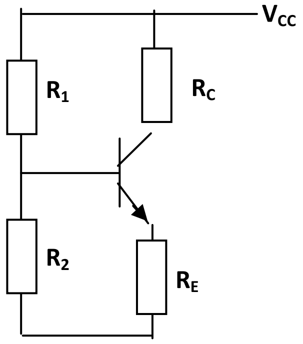


Figure 4-40 : Circuit for Exercise 04.3

Exercise 04.4 : Voltage Divider Bias (CE configuration)

The transistor of Figure 4-41 has the following set of h parameters:

$h_{11} = 100\Omega; h_{21} = 100;\ h_{12} = h_{22}^{-1} = 0$

With m:

$R_1 = 33K\Omega; R_2 = 10K\Omega;\ R_C = R_L = 3.3K\Omega;\ R_{E1} =;\ R_{E2} = 330\Omega$

- Give the type of amplifier of the circuit.
- Calculte G_V Z_I and Z_O

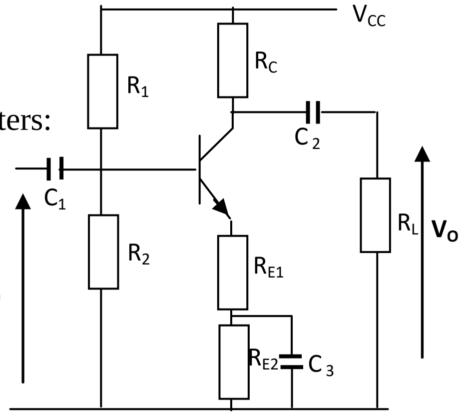


Figure 4-41 : Circuit for Exercise 04.4

Exercise 04.5 : Voltage Divider Bias (CB configuration)

The transistor of Figure 4-42 has the following set of h parameters:

$h_{11} = 800\Omega; h_{21} = 80;\ h_{12} = 0\ and\ h_{22}^{-1} = 20K\Omega$

With $R_B = R_1 // R_2 = 4.91K\Omega;\ R_C = R_L = 3.33K\Omega\ and\ R_E = 667\Omega$

- Give the type of amplifier of the circuit.
- Calculte G_V Z_I and Z_O

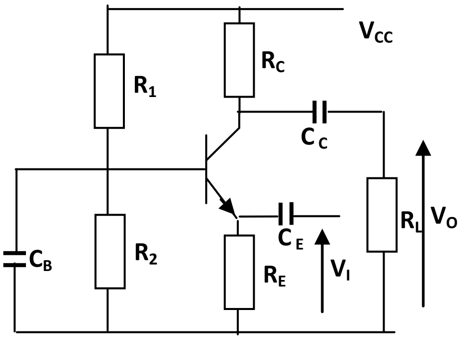


Figure 4-42 : Circuit for Exercise 04.5

Exercise 04.6 : Voltage Divider Bias (CC configuration)

The transistor of Figure 4-43 has the following set of h parameters:

$h_{11} = 1000\Omega; h_{21} = 120;\ h_{12} = 0\ and\ h_{22}^{-1} = 25K\Omega$

With $R_B = R_1 // R_2 = 1.83K\Omega;\ R_C = R_L = 400\Omega$

- Give the type of amplifier of the circuit.
- Calculte G_V Z_I and Z_O

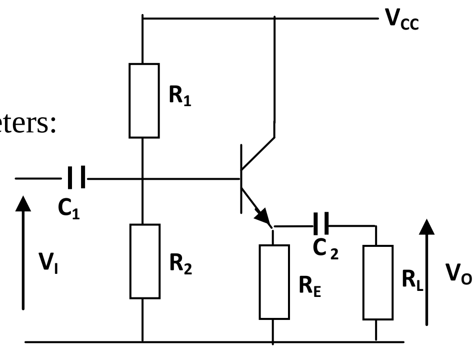


Figure 4-43 : Circuit for Exercise 04.6

Exercise 04.7 : Two-transistor NPN Darlington

The so-called "Darlington" transistor is made up of two transistors (both NPN, both PNP, or a combination of the two types). The circuit is given in Figure 4-44

The hybrid parameters of transistor T_1 are: $h_{11} = 1K\Omega; h_{12} = h_{22} 00\ et\ h_{21} = \beta_1 = 30$

The hybrid parameters of transistor T_2 are: $h'_{11} = 1K\Omega; h'_{12} = h'_{22} = 0\ et\ h'_{21} = \beta_2 = 100$

1. Neglecting leakage currents, determine (in DC) the current gain of the equivalent transistor and the base-emitter potential difference : $V_{BE1} = V_{BE2} = 0,7V$
2. Give the small-signal equivalent circuit of the configuration.

3. Calculate the input resistance. $R_i = \dfrac{V_{be}}{i_b}$

4. What is the advantage (purpose) of this configuration?

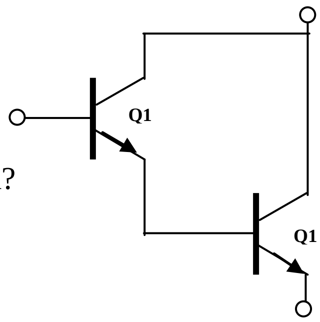


Figure 4-44 : Circuit for Exercise 04.7

Exercise 04.8 : Cascode Connection

The two transistor T_1 and T_2 of Figure 4-45 has the following the same dynamic parameters :

$$T_1 : h_{11_1} = h_{11_2} = 1200\Omega; h_{21_1} = h_{21_2} = 100\Omega; T_2 = h_{12_1} = h_{12_2} = 0; h_{22_1} = h_{22_2} = 0$$

With

$$R_1 = 52K\Omega; R_2 = 36{,}4K\Omega,\ R_3 = 18K\Omega\ , R_C = 3K\Omega\ \ and\ R_E = 1K\Omega$$

1- Determine the type of circuit for each transistior and give the small-signal equivalent circuit of the configuration

2- The total gain for the system, Av and Avs.

3- Calculate the input impedance of the second stage

4- The total gain for the system G_v

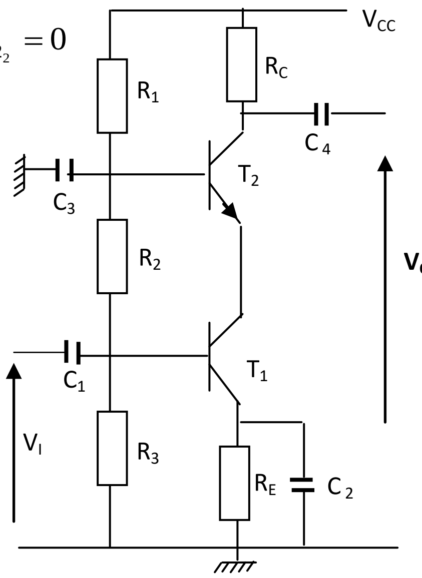


Figure 4-45 : Circuit for Exercise 04.8

Exercise 04.9 : The BJI as a switch

(1)- For the transistor circuit in Figure 4-46, what is V_{CE} when V_{IN} = 0 V?

(2)- What minimum value of I_B is required to saturate this transistor if β_{DC} is 200? Neglect $V_{CE(sat)}$.

(3) - Calculate the maximum value of R_B when V_{IN} = 5 V.

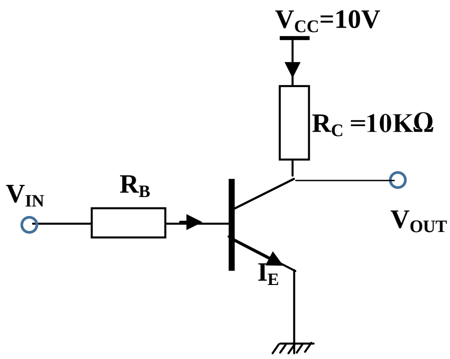


Figure 4-46 : Circuit for Exercise 04.9

BIPOLAR JUNCTION TRANSISTOR (BJT)

Solutions

Exercise 04.1 : Emitter Bias

From Figure 4-38

Given

$\beta = 80;\ R_B = 10K\Omega.; R_C = 325\Omega; RE = 200\Omega; V_{CC} = 25V$ and $V_{BE} = 0.7V$

Value of collector current

Using Equation 4.16, the collector current is

$$V_{CC} = R_B I_B + V_{BE} + R_C I_C$$

$$V_{CC} = R_B \frac{I_C}{\beta} + V_{BE} + R_C I_C$$

$$V_{CC} = \left(\frac{R_B}{\beta} + R_C\right) I_C + V_{BE}$$

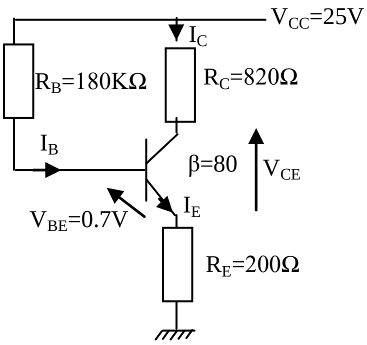


Figure :4.38

$$I_{C0} + I_{B0} + I_2$$

Value of collector to emitter voltage

$$V_{CC} = (R_E + R_C) I_C + V_{CE} \Rightarrow V_{CE} = V_{CC} - (R_E + R_C) I_C$$

$$V_{CE} = 25 - (200 + 820) 9.9 \times 10^{-3} = 14.9V$$

Exercise 04.2 : Emitter Bias

Calculation of the coordinates I_{C0} and V_{CE0}.

The equations of the circuit are:

$$V_{CC} = R_C (I_{C0} + I_1) + V_{CE0}$$

$$V_{BE0} = R_2 I_2 \Rightarrow I_2 = \frac{V_{BE0}}{R_2} = \frac{0.7}{3 \times 10^3} = 0.233mA$$

$$V_{CC} = R_C (I_{C0} + I_1) + R_1 I_1 + R_2 I_2$$

$$V_{CC} = R_C (\beta I_{B0} + I_{B0} + I_2) + R_1 (I_{B0} + I_2) + R_2 I_2$$

$$V_{CC} = R_C ((\beta + 1) I_{B0} + I_2) + R_1 (I_{B0} + I_2) + R_2 I_2$$

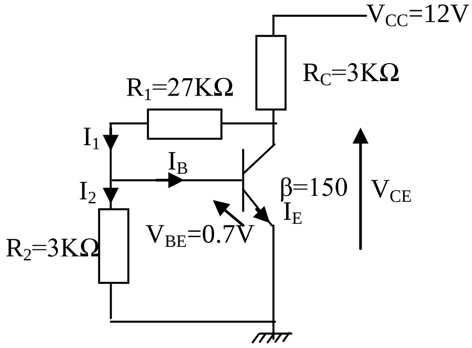


Figure :4.39

$$V_{CC} = (R_C + R_1 + R_2)I_2 + (R_C(\beta+1) + R_1)I_{B0}$$

$$I_{B0} = \frac{V_{CC} - (R_C + R_1 + R_2)I_2}{R_C(\beta+1) + R_1} = \frac{12 - (33\times10^3)0.233\times10^{-3}}{3\times10^3(1+100) + 27\times10^3} = 13.06\mu A$$

$$I_{CO} = \beta I_{B0} = 100\times13.06\times10^{-6} = 1.306 mA$$

$$I_1 = I_{B0} + I_2 = 0.233\times10^{-3} + 13.06\times10^{-6} = 0.246 mA$$

Value of collector to emitter voltage

$$V_{CC} = (I_{C0} + I_1)R_C + V_{CE} \Rightarrow V_{CE} = V_{CC} - (I_{C0} + I_1)R_C$$

$$V_{CE} = 12 - (0.246 + 1.306)3 = 7,344V$$

The coordinates of the operating point are: (1.306 mA, 7.344 V)

Exercise 04.3: Voltage-divider configuratin

Calculation of the coordinates I_{C0} and V_{CE0}.

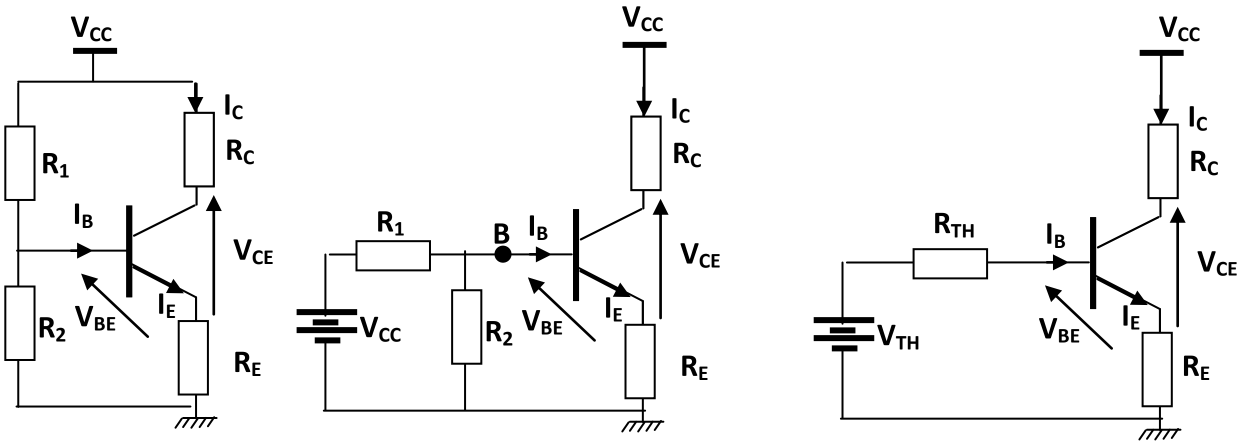


Figure 4.40.a: Thevenizing the bias circuit.

This example tests how much the Q-point will shift if the level of b is cut in half rather than comparing exact and approximate methods. E_{Th} and R_{Th} are identical:

For $\beta=100$

From (E.q 4.39)

$$R_{TH} = \frac{R_1\times R_2}{R_1 + R_2} = \frac{3,39\times39\times10^6}{(3,39+39)\times10^3} = 3,55K\Omega$$

From (E.q 4.40)

$$E_{TH} = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{3,9\times10^3\times22}{(3,9+39)10^3} = 2V$$

From (E.q 4.43)

$$I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + R_E(1+\beta)} = \frac{2-0,7}{3,55\times10^3 + 1,5\times10^3(100+1)} = 8,38\mu A$$

From (E.q 4.11)

$$I_{CQ} = \beta I_B = 100\times8,38\times10^{-6} = 0,84mA$$

From (E.q 4.47)

$$V_{CC} = V_{CEQ} + (R_C + R_E)I_C \Rightarrow V_{CE} = V_{CC} - (R_C + R_E)I_C$$

$$V_{CEQ} = 22 - (10+1,5)10^3 \times 0,84\times10^{-3} = 12,34V$$

For $\beta = 50$

From (E.q 4.43)

$$I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + R_E(1+\beta)} = \frac{2-0,7}{3,55\times10^3 + 1,5\times10^3(50+1)} = 16,24\mu A$$

From (E.q 4.11)

$$I_{CQ} = \beta I_B = 50\times16,24\times10^{-6} = 0,81mA$$

From (E.q 4.47)

$$V_{CC} = V_{CEQ} + (R_C + R_E)I_C \Rightarrow V_{CE} = V_{CC} - (R_C + R_E)I_C$$

$$V_{CEQ} = 22 - (10+1,5)10^3 \times 0,81\times10^{-3} = 12,69V$$

After tabulating the outcomes, we have

Impact of b change on the voltage-divider configuration's response in Figure 4-40.a

β	$I_{CQ}(mA)$	$V_{CEQ}(mA)$
100	**0,84**	**12,61**
50	**0,81**	**12 ,69**

The circuit's relative insensitivity to the change non β is evident from the results, which demonstrate that even when b is significantly reduced from 100 to 50, the values of I_{CQ} and V_{CEQ} remain nearly unchanged.

Exercise 04.4 : Voltage Divider Bias (CE configuration)

1- **The type of amplifier of the circuit**.

Input : Base

Output : Collector : A common-emitter amplifier

Calculte G_V

Figure 4-41 shown the equivalent circuit for the common-emitter amplifier

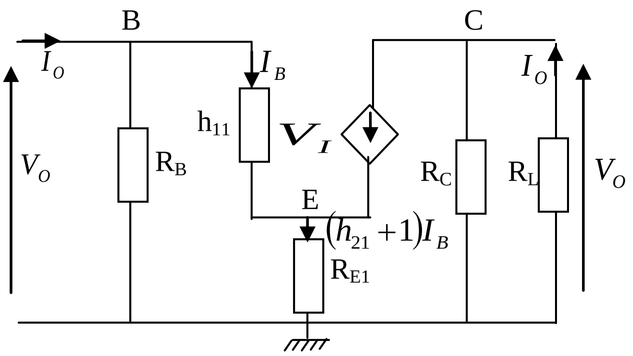


Figure 4-41.a

Voltage gain

$$G_V = \frac{V_O}{V_I} \quad V_O = -(R_C // R_L)h_{21}I_B$$

$$V_I = [h_{11} + R_{E1}(h_{21}+1)]I_B$$

$$G_V = -\frac{(R_C // R_L)h_{21}I_B}{V_I = [h_{11} + R_{E1}(h_{21}+1)]I_B}$$

$$G_V = -\frac{(R_C // R_L)h_{21}}{h_{11} + R_{E1}(h_{21}+1)} = \frac{\frac{3.3\times 3.3\times 10^6}{(3.3+3.3)10^3}\times 175}{20+330(175+1)} = \frac{-288750}{58\ 100} = -4.96$$

Input Impedance $Z_I = \frac{V_I}{I_I}$

$$V_I = R_B(I_I - I_B)$$

$$V_I = (h_{11} + R_{E1}(h_{21}+1))I_B$$

$$V_I = R_B\left(i_e - \frac{V_e}{(h_{11} + R_{E1}(h_{21}+1))}\right)$$

$$V_I[h_{11} + R_{E1}(h_{21}+1) + R_B] = I_I[(h_{11} + R_{E1}(h_{21}+1))R_B]$$

$$Z_I = \frac{V_I}{I_I} = \frac{(h_{11} + R_{E1}(h_{21}+1))\times R_B}{h_{11} + R_{E1}(h_{21}+1) + R_B} = \frac{(20+330(175+1))\times 5\times 10^3}{(20+330(175+1))+5\times 10^3} = \frac{290\ 500}{63\ 100} = 4603\Omega$$

Current gain $G_I = \frac{I_O}{I_I}$

From equation 4.59

$$G_I = -G_V \frac{Z_I}{R_L} = 4.96 \frac{4603}{3.3 \times 10^3} = 6.91$$

Ouput Impedance $Z_O = \frac{V_O}{I_O}$

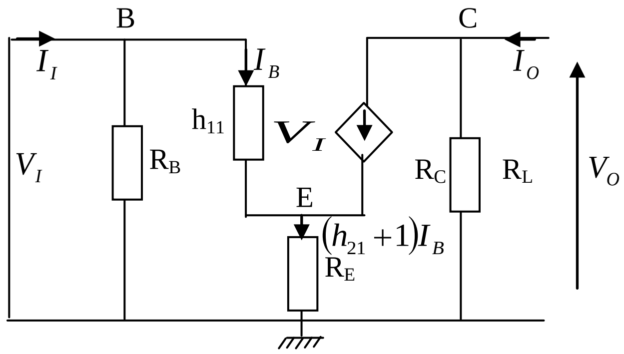


Figure 4-41.b

We use Thévenin's theorem:

• Disconnect the load

• Short-circuit the generator at the input V_I=0

• Apply a voltage Vs at the output, which injects a current I_O

$$V_I = 0 \Rightarrow i_b = 0 \Rightarrow i_C = h_{21}\, i_b = 0$$

$$V_O = R_C(i_S - h_{21} i_b) = R_C i_S \Rightarrow Z_S = R_C = 3.3K\Omega$$

Exercise 04.5 : Voltage Divider Bias (CB configuration)

1-**The type of amplifier of the circuit**.

Input : Emitter

Output : Collector : A common-Base amplifier

Figure 4-42.a shown AC the equivalent circuit for Common-base amplifier

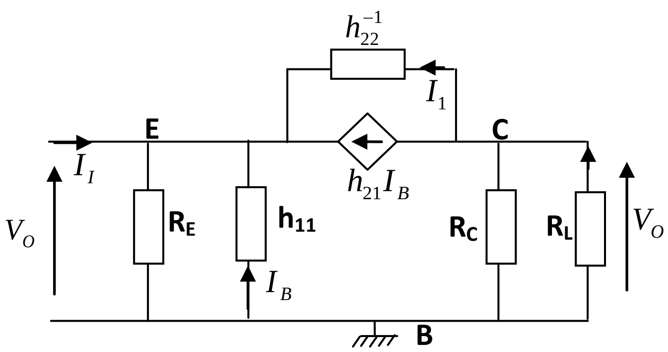


Figure 4-42.a

2- **Calculte G_V**

$$A_V = G_V = \frac{V_S}{V_e};$$

$$V_I = -h_{11} i_b \Rightarrow i_b = -\frac{V_I}{h_{11}} \qquad V_I = -h_{22}^{-1} i_1 + V_O \Rightarrow i_1 = \frac{V_O - V_I}{h_{22}^{-1}}$$

$$V_O = -(R_L // R_C)(h_{21} i_b + i_1)$$

$$V_O = -(R_L // R_C)\left(-\frac{V_I h_{21}}{h_{11}} + \frac{V_O - V_I}{h_{22}^{-1}}\right)$$

$$V_O\left(1 + \frac{(R_L // R_C)}{h_{22}^{-1}}\right) = V_I\left(\frac{(R_L // R_C)h_{21}}{h_{11}} + \frac{1}{h_{22}^{-1}}\right)$$

$$\frac{V_O}{V_I} = \frac{\left(\frac{(R_L // R_C)h_{21}}{h_{11}} + \frac{1}{h_{22}^{-1}}\right)}{\left(1 + \frac{(R_L // R_C)}{h_{22}^{-1}}\right)} = \frac{\frac{(R_L // R_C)h_{21}h_{22}^{-1} + h_{11}}{h_{11}h_{22}^{-1}}}{\frac{h_{22}^{-1} + (R_L // R_C)}{h_{22}^{-1}}}$$

$$= \frac{(R_L // R_C)h_{21}h_{22}^{-1} + h_{11}}{h_{11}h_{22}^{-1}} \times \frac{h_{22}^{-1}}{h_{22}^{-1} + (R_L // R_C)}$$

$$G_V = \frac{(1.67\times10^3)80\times20000+800}{20000\times800} \times \frac{20000}{20000+(1.67\times10^3)} = \frac{53\,440\,016\times10^6}{346\,72\times10^7} = 154$$

Input Impedance $Z_I = \frac{V_I}{I_I}$

$V_O = -h_{11} i_b$ $\qquad V_e = (R_E // h_{11})(i_e + i)$

$$i = i_1 + h_{21} i_b$$

$$V_O = (R_E // h_{11})\left(i_I + \frac{V_O - V_I}{h_{22}^{-1}} - \frac{h_{21}V_I}{h_{11}}\right) \qquad G_V = \frac{V_O}{V_I} \Rightarrow V_O = G_V V_I$$

$$V_I = (R_E // h_{11})\left(i_I + \frac{(G_V - 1)V_I}{h_{22}^{-1}} - \frac{h_{21}V_I}{h_{11}}\right)$$

$$\left(1 + (R_E // h_{11})\left(\frac{-G_V + 1}{h_{22}^{-1}} + \frac{h_{21}}{h_{11}}\right)\right)V_I = (R_E // h_{11})i_I$$

$$Z_I = \frac{V_I}{i_{Ie}} = \frac{(R_E // h_{11})}{\left(1 + (R_E // h_{11})\left(\frac{-G_V + 1}{h_{22}^{-1}} + \frac{h_{21}}{h_{11}}\right)\right)} = \frac{363}{(1+363)\left(\frac{-154+1}{20000} + \frac{80}{800}\right)} = \frac{363}{33.6154} = 10.79\Omega$$

Current Gain e G_i **;**

$$G_i = \frac{i_O}{i_I} \qquad \left.\begin{matrix} V_O = -R_L i_O \\ V_I = Z_I i_I \end{matrix}\right\} \Rightarrow \frac{i_O}{i_I} = -\frac{V_O Z_I}{R_L V_I} = -\frac{Z_I}{R_L} G_v = \frac{154\times10{,}79}{3{,}33\times10^3} = -0.498$$

Ouput Impedance $Z_O = \frac{V_O}{I_O}$

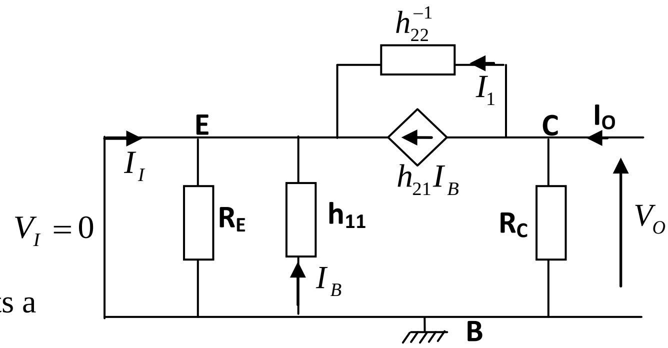


Figure 4-42.b

We use Thévenin's theorem:

- Disconnect the load
- Short-circuit the generator at the input V_I=0
- Apply a voltage Vs at the output, which injects a current I_O

$$V_0 = R_C\left(i_O - \left(i_1 + h_{21}i_b\right)\right) \quad \text{avec } V_I = 0 \Rightarrow h_{21}i_b = 0$$

$$V_O = R_C\left(i_O - i_1\right) \quad i_1 = \frac{V_O - V_I}{h_{22}^{-1}}$$

$$V_O = R_C\left(i_I - \frac{V_O}{h_{22}^{-1}}\right) = R_C i_I - \frac{R_C V_O}{h_{22}^{-1}} \Rightarrow V_O + \frac{R_C V_O}{h_{22}^{-1}} = R_C i_O$$

$$V_O\left(1 + \frac{R_C}{h_{22}^{-1}}\right) = R_C i_O \Rightarrow Z_O = \frac{V_O}{i_O} = \frac{R_C}{1 + \frac{R_C}{h_{22}^{-1}}} = \frac{3{,}33\times10^3}{1 + \frac{3{,}33\times10^3}{20\times10^3}} = 2{,}85K\Omega$$

Exercise 04.6: Voltage Divider Bias (CC configuration)

1-**The type of amplifier of the circuit**.

Input : Base

Output : Emitter : A common-Collector amplifier

Figure 4-43.a shown AC the equivalent circuit for Common-base amplifier

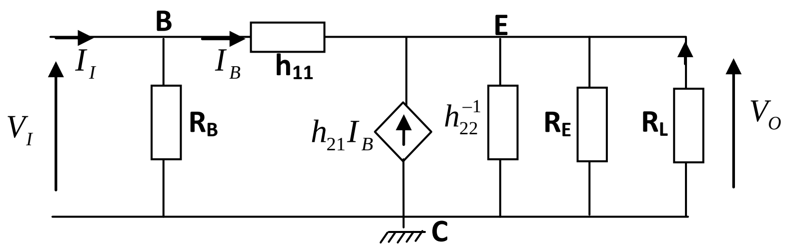


Figure 4-43.a :

Voltage gain $G_V = \frac{V_O}{V_I}$

$$V_O = \left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21} + 1\right)I_B$$

$$V_I = h_{11} I_B + V_O$$

$$V_I = \left[h_{11} + \left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21}+1\right)\right] I_B$$

$$G_V = \frac{\left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21}+1\right) I_B}{\left[h_{11} + \left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21}+1\right)\right] I_B}$$

$$G_V = \frac{\left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21}+1\right)}{\left[h_{11} + \left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21}+1\right)\right]} = \frac{R\left(h_{21}+1\right)}{\left[h_{11} + R\left(h_{21}+1\right)\right]}$$

$$R = \frac{R_E \times R_L \times h_{22}^{-1}}{R_E \times R_L + R_L \times h_{22}^{-1} + R_E \times h_{22}^{-1}} = \frac{400 \times 400 \times 25000}{400 \times 400 + 400 \times 25000 + 400 \times 25000} = \frac{4 \times 10^9}{2016 \times 10^4} = 198$$

$$G_V == \frac{R\left(h_{21}+1\right)}{\left[h_{11} + R\left(h_{21}+1\right)\right]} = \frac{198(120+1)}{1000+198(120+1)} = \frac{23\,958}{24\,958} = 0.95 \approx 1$$

Input Impedance $Z_I = \dfrac{V_I}{I_I}$

$$V_I = R_B\left(I_I - I_B\right)$$

$$V_I = \left[h_{11} + \left(R_E // R_L // h_{22}^{-1}\right)\left(h_{21}+1\right)\right] I_B$$

$$I_B = \frac{V_I}{h_{11} + \left(h_{21}+1\right)\left(R_E // R_L / h_{22}^{-1}\right)}$$

$$V_I = R_B\left(I_I - \frac{V_I}{h_{11} + \left(h_{21}+1\right)\left(R_E // R_L / h_{22}^{-1}\right)}\right)$$

$$V_I\left[h_{11} + \left(h_{21}+1\right)\left(R_E // R_L / h_{22}^{-1}\right) + RB\right] = I_I\left[\left(h_{11} + \left(h_{21}+1\right)\left(R_E // R_L / h_{22}^{-1}\right)\right) RB\right]$$

$$Z_I = \frac{V_I}{I_I} = \frac{\left(h_{11} + \left(h_{21}+1\right)\left(R_E // R_L / h_{22}^{-1}\right)\right) RB}{h_{11} + \left(h_{21}+1\right)\left(R_E // R_L / h_{22}^{-1}\right) + RB}$$

$$Z_I = \frac{\left(1000 + (120+1)(198)\right) 1.83 \times 10^3}{\left(1000 + (120+1)(198)\right) + 1.83 \times 10^3} = \frac{45\,673{,}14}{24\,959{,}83} = 1.82\Omega$$

Ouput Impedance $Z_O = \dfrac{V_O}{I_O}$

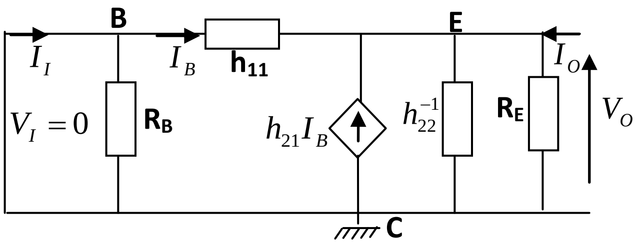


Figure 4-43.b

We use Thévenin's theorem:

- Disconnect the load
- Short-circuit the generator at the input V_I=0
- Apply a voltage V_O at the output, which injects a current I_O

$$V_O = \left(R_E // h_{22}^{-1}\right)\left(I_O + \left(h_{21}+1\right)I_B\right)$$

$$V_O = 0 \Rightarrow h_{11}I_B + V_O \Rightarrow I_B = -\frac{V_O}{h_{11}}$$

$$V_O = \left(R_E // h_{22}^{-1}\right)\left(I_O - \left(h_{21}+1\right)\frac{V_O}{h_{11}}\right) \Rightarrow V_O(1+\left(h_{21}+1\right)\frac{\left(R_E // h_{22}^{-1}\right)}{h_{11}}) = \left(R_E // h_{22}^{-1}\right)I_O$$

$$Z_O = \frac{V_O}{I_O} = \frac{\left(R_E // h_{22}^{-1}\right)h_{11}}{h_{11} + \left(h_{21}+1\right)\left(R_E // h_{22}^{-1}\right)} = \frac{\left(\frac{1000\times 400}{1000+400}\right)120}{1000+\left(120+1\right)\times 285,} = \frac{34\,285}{35\,485} = 0.96\Omega$$

Exercise 04.7 : Two-transistor NPN Darlington

1-The current gain

In DC operation, the current flowing through the collector is:

$$I_C = I_{C1} + I_{C2}$$

$$I_C = \beta_1 I_{B1} + \beta_2 I_{B2}$$

$$I_{B1} = I_{E1} = I_{C1} + I_B = \beta_1 I_B + I_B = \left(\beta_1 + 1\right)I_B$$

$$I_C = \beta_1 I_B + \beta_2\left(\beta_1 + 1\right)I_B$$

$$I_C = \beta_1 I_B + \beta_2\beta_1 I_B + \beta_2 I_B$$

$$I_C = \left(\beta_1 + \beta_2\beta_1 + \beta_2\right)I_B$$

$$\beta_2 = \beta_1$$

$$I_C = \left(\beta^2 + 2\beta\right)I_B$$

$$\beta^2 \succ\succ 2\beta$$

$$I_C \approx \beta^2 I_B$$

2- The potential difference between the base and the emitter is:

$$V_{BE} \approx 0{,}7 + 0{,}7 = 1{,}4V$$

3- Small-signal quivalent circuit

The dynamic equivalent circuit of the configuration in small-signal operation and at low frequencies is shown in the Figure 4-44.a.

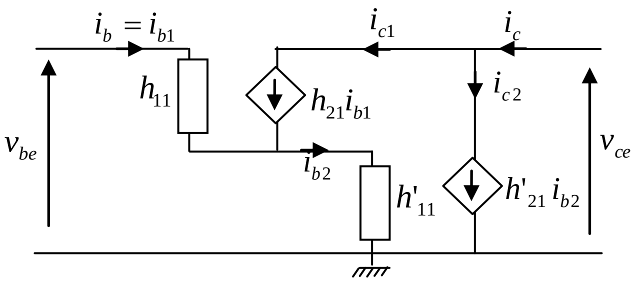


Figure 4.44.a

4- input resistance

$$v_{be} = h_{11}i_{b1} + h'_{11}\,i_{b2}$$

D'aprés la loi des noeud on a:

$$i_{b2} = h_{21}i_{b1} + i_{b1} = i_{b1}(1+h_{21}) \qquad i_b = i_{b1}$$

$$v_{be} = [h_{11} + h'_{11}\,(1+h_{21})]i_b = r_e i_b$$

$$r_e = \frac{v_{be}}{i_b} = [h_{11} + h'_{11}\,(1+h_{21})] = [1000+1000(1+30)] = 41K\Omega$$

5- The Darlington configuration significantly improves the input resistance as well as the current gain. This configuration is generally used as a power stage at the output of an amplifier.

Exercise 04.8 : Cascode Connection

1-**The type of amplifier of the circuit**.

T_1 :Input : Base

Output : Collector : Common-emitter amplifier

T_2 :Input : Emitter

Output : Collector : Common-Base amplifier

2-Small-signal quivalent circuit

The dynamic equivalent circuit of the configuration in small-signal operation and at low frequencies is shown in the Figure 4-45.a.

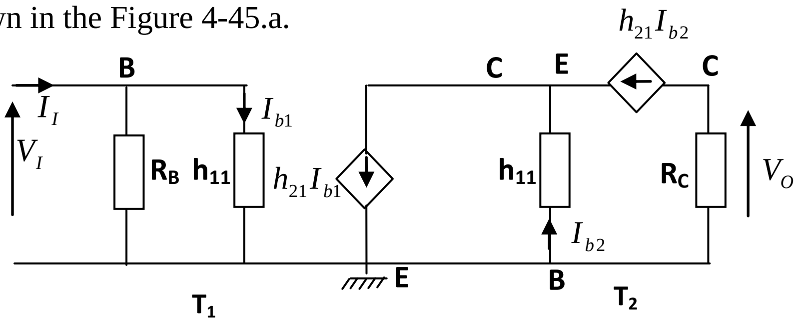


Figure 4 .45.a

Voltage gain

$$G_{V2} = \frac{V_O}{V_{I2}}$$

$$V_O = -R_C h_{21} ib_2$$

$$V_{I2} = -h_{11} ib_2$$

$$G_{V2} = \frac{R_C h_{21} ib_2}{h_{11} ib_2} = \frac{R_C h_{21}}{h_{11}} = - = 250$$

The input impedance of the second stage is

$$Z_{I2} = \frac{V_{I2}}{I_{I2}}$$

$$I_{I2} = -(h_{21}+1) i_{b2} = \frac{(h_{21}+1)}{h_{11}} V_{I2}$$

$$Z_{I2} = \frac{V_{I2}}{\frac{(h_{21}+1)}{h_{11}} V_{I2}} = \frac{h_{11}}{h_{21}+1} = \frac{1200}{100} = 12\Omega$$

Voltage gain

$$G_{V1} = \frac{V_{O1}}{V_I}$$

$$V_I = h_{11} i_{b1}$$

$$V_{O1} = -Z_{I2} h_{21} i_{b1}$$

$$G_{V1} = \frac{-Z_{I2} h_{21} i_{b1}}{h_{11} i_{b1}} = \frac{-h_{21} Z_{I2}}{h_{11}} = \frac{-h_{21}}{h_{11}} \frac{h_{11}}{h_{21}+1} = -\frac{h_{21}}{h_{21}+1} = -\frac{100}{101} = -0{,}99$$

Voltage gain

$$G_V = G_{V1} \times G_{V2} = 250 \times 0{,}99 = -248$$

Exercise 04.9 : The BJI as a switch

(1)- When V_{IN}=0, the transistor is in cutoff (acts like an open switch) and

$$V_{CE} = V_{CC} = 10V$$

(2)- Since $V_{CE(sat)}$ is neglected (assumed to be 0 V),

$$I_{C(SAT)} = \frac{V_{CC}}{R_C} = \frac{10}{10 \times 10^3} = 10mA$$

$$I_{B(\min)} = \frac{I_{C(SAT)}}{\beta_{DC}} = \frac{10\times10^{-3}}{200} = 50\mu A$$

(3)- When the transistor is on VBE=0,7 V, The voltage across R_B is

$$V_{RB} = V_{IN} - V_{BE} = 5 - 0,7 = 4,3V$$

Calculate the maximum value of R_B

$$R_B = \frac{V_{RB}}{I_{B\min}} = \frac{4,3}{50\mu A} = 86\,\text{K}\Omega$$

Chapter 05

OPERATIONL AMPLIFIERS

(Op-Amp)

5 OPERATIONL AMPLIFIERS (Op-Amp)

Learning Objectives

By studying this chapter and completing the related exercises, you will be able to:

1. Understand the concept and operation of Operational Amplifiers (Op-Amps).
2. Identify the pin configuration (pinout) and circuit symbol of an operational amplifier.
3. Understand the relationship between the output voltage (V_O) and the differential input voltage (V_d).
4. Analyze the equivalent circuit of a non-ideal operational amplifier.
5. Understand the main operational amplifier configuration topologies.
6. Analyze the behavior and applications of different Op-Amp circuits.
7. Understand the basic characteristics and limitations of practical operational amplifiers.

5.1 What is Operationl Amplifier ?

An **Op-Amp** is an active circuit element designed to perform mathematical operations of Amplification, Addition (Summing)**,** subtraction, differentiation, integration, comparison, filtering and oscillation…..etc

Figure 5-1 shows one of the most famous operation amplifiers which is known as 741 Op-Amp.

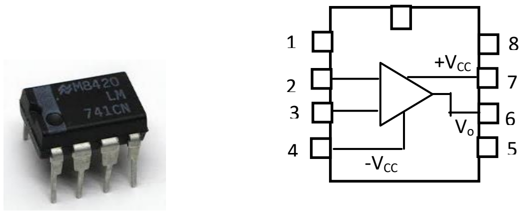


Figure 5-1 : Pin configuration

Figure 5-1 illustrates a typical op-amp package. The eight terminals are:

1- Balance
2- Inverting input
3- Noninverting input
4- The negative power supply V^-
5- Balance
6- Output
7- The positive power supply V^+
8- No connection

5.2 Circuit Symboles

The standard operational amplifier (Op-Amp) symbol is shown in figure 5-2:

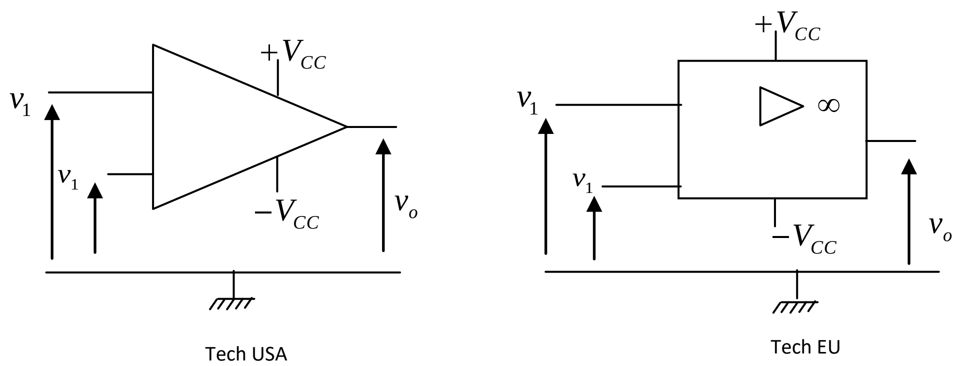


Figure 5-2 : Circuit Symboles

5.3 The equivalent circuit of an Op-Amp

The equivalent circuit model of an Op-Amp is illustrated in figure. 5-3. The output stage is represented by a voltage-controlled source in series with the output resistance R_o. As shown in figure 5-3, the input resistance Ri corresponds to the Thevenin equivalent resistance observed at the input terminals, while the output resistance R_o represents the Thevenin equivalent resistance observed at the output.

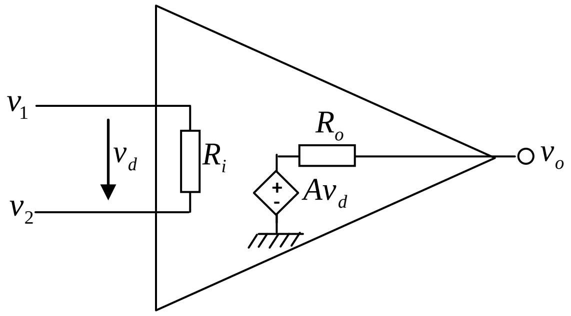


Figure 5-3 : The equivalent circuit of the nonideal Op-Amp

The differential input voltage v_d can be expressed as:

$$v_d = v_2 - v_1 \quad (5.1)$$

The output voltage vo is given by

$$v_o = Av_d = A(v_2 - v_1) \quad (5.2)$$

where

A: is called the open-loop voltage gain

v_1: is the voltage between the inverting terminal and ground

v_2 : is the voltage between the noninverting terminal and ground

5.4 Typical ranges for Op-Amp parameters

Table 5-1 illustrates that the typical ranges for Op-Amp parameters

Table 5-1 : Typical ranges for Op-Amp parameters

Parameter	Typical range	Ideal values
Open-loop gain A	10^5 *to* $10^8 \Omega$	∞
Input resistance R_i	10^6 *to* $10^{13} \Omega$	∞
Output resistance R_o	10 *to* 100Ω	0
Supply voltage V_{CC}	5 *to* $24V$	-

Op-Amp output voltage V_O as a function of the differential input voltage V_d

Figure 5-4 illustrates that the Op-Amp can operate in three modes, depending on the differential input voltage vd:

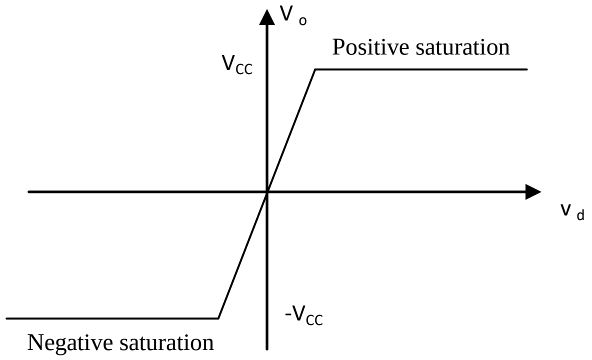


Figure 5-4 : Op-Amp output voltage Vo as a function of the differential input voltage vd

- **Positive saturation,** $V_O = V_{CC}$
- Linear region : $-V_{CC} \le V_O = AV_d \le V_{CC}$
- **negative saturation:** $V_O = V_{CC}$

If we attempt to increase v_d beyond the linear range, the Op-Amp becomes saturated and yields Vo= V_{CC} or Vo= -V_{CC} (used in camparators). Throughout this book, we will assume that our op amps operate in the linear mode. This means that the output voltage is restricted by

$$-V_{CC} \le V_O \le V_{CC} \qquad (5.3)$$

Although we shall always operate the Op-Amp in the linear region, the possibility of saturation must be borne in mind when one designs with op amps, to avoid designing Op-Amp circuits that will not work in the laboratory.

5.5 Operational Amplifier Configuration Topologies

There are several different Op-Amp circuits, each differing in function. The most common topologies are described below.

5.5.1 ideal Op- Amp

An ideal Op-Amp is an amplifier with infinite open-loop gain, infinite input resistance, and zero output resistance

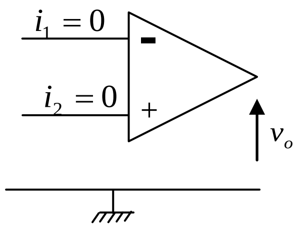


Figure 5-5 : Ideal Op-Amp

Two important characteristics of the ideal Op-Amp are:

- The **currents** into both input terminals are **zero**:

$$i_1 = i_2 = 0 \tag{5.4}$$

- The **voltage** across the input terminals is equal to **zero**

$$V_d = V^+ - V^- = 0 \Rightarrow V^+ = V^- \tag{5.5}$$

5.5.2 Inverting Amplifier

The fundamental inverting amplifier configuration is illustrated in figure 5-6. The input signal, V_I is applied to the inverting terminal, while the rest of the circuit is composed of resistors R_1 and R_f.

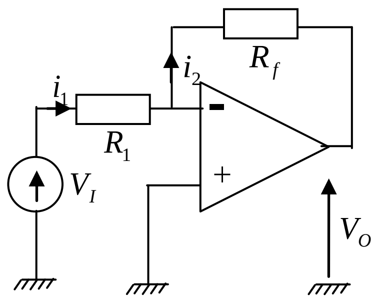


Figure 5-6 : The Inverting Amplifier

$$Ad = \infty \Rightarrow i_1 = i_2 \tag{5.6}$$

$$V_1 - V^- = R_1 i_1 \Rightarrow i_1 = \frac{V_1 - V^-}{R_1} \tag{5.7}$$

$$V^- - V_O = R_{f-} i_2 \Rightarrow i_2 = \frac{V \;\; - V_O}{R_f} \tag{5.8}$$

But $V^- = V^+ = 0$ for an ideal op amp, since the noninverting terminal is grounded. Hence,

$$\frac{V_1}{R_1} = -\frac{V_O}{R_f} \Rightarrow V_O = -\frac{R_f}{R_1} V_1 \tag{5.9}$$

An inverting amplifier reverses the polarity of the input signal while amplifying it

5.5.3 Noninverting amplifier

Figure 5-7 shows the basic non-inverting amplifier configuration. The negative feedback is maintained and the input signal is now applied to the non-inverting terminal

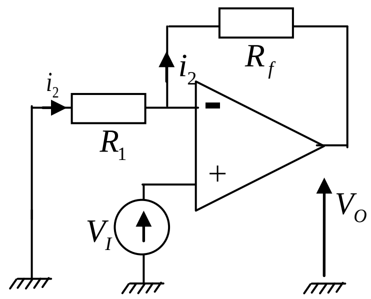


Figure 5-7 : Non-inverting Amplifier

Application of KCL at the inverting terminal gives

$$i_1 = i_2 \tag{5.10}$$

$$0 - V^- = R_1 i_1 \Rightarrow i_1 = \frac{0 - V^-}{R_1} \tag{5.11}$$

$$V^- - V_O = R_f i_2 \Rightarrow i_2 = \frac{V^- - V_O}{R_f} \tag{5.12}$$

But $V^- = V^+ = V_I$

$$\frac{V_I}{R_1} = \frac{V_I - V_O}{R_f} \Rightarrow R_1 (V_I - V_O) = R_f V_I \tag{5.13}$$

$$-R_1 V_O = -(R_f + R_1) V_I \tag{5.14}$$

$$V_O = \left(1 + \frac{R_f}{R_1}\right) V_I \tag{5.15}$$

A **non-inverting** amplifier is an Op-Amp circuit designed to provide a positive voltage gain.

5.5.4 Voltage follower

An operational amplifier (op-amp) design in which the output voltage directly follows (or equals) the input voltage is called a **voltage follower**, sometimes referred to as a **buffer amplifier** or unity gain amplifier.

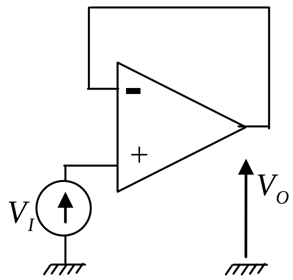


Figure 5-8 : Op-amp Voltage follower

$$V_O = V_I \tag{5.16}$$

5.5.5 Summing Op-Amp

A **summing amplifier** is an Op-Amp circuit that combines several inputs and produces an output that is the weighted sum of the input

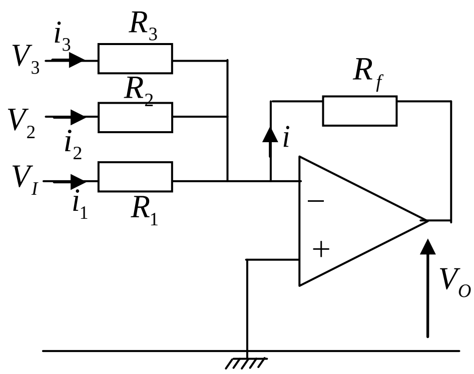


Figure 5-9 : Summing Op-Amp

Application of KCL at the inverting terminal gives

$$i = i_1 + i_2 + i_3 \tag{5.17}$$

$$V^- = V^+ = 0 \tag{5.18}$$

$$V_1 - V^- = R_1 i_1 \Rightarrow i_1 = \frac{V_1 - V^-}{R_1} \tag{5.19}$$

$$V_2 - V^- = R_2 i_2 \Rightarrow i_2 = \frac{V_2 - V^-}{R_2} \tag{5.20}$$

$$V_3 - V^- = R_3 i_3 \Rightarrow i_3 = \frac{V_3 - V^-}{R_3} \tag{5.21}$$

We note that $V^- = V^+ = 0$ and substitute Eq. (5.14) into Eq. (5.13). We get

$$V_o = -R_f i = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) \tag{5.22}$$

$$R_1 = R_2 = R_3 \Rightarrow V_0 = -(V_1 + V_2 + V_3) \tag{5.23}$$

5.5.6 Difference Amplifier

A difference amplifier is a device that amplifies the difference between two inputs but rejects any signals common to the two inputs

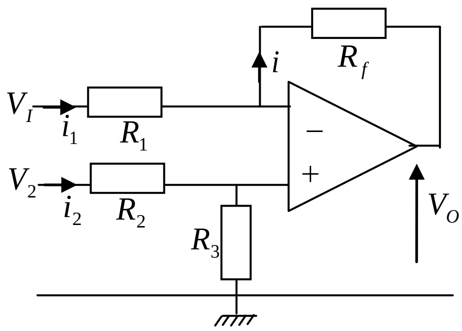


Figure 5-10 : Difference Amplifier

Consider the Op-Amp circuit shown in figure. 5-10. Keep in mind that zero currents enter the Op-Amp terminals. Applying KCL to node a,

$$\frac{V_1 - V^-}{R_1} = \frac{V^- - V_0}{R_f} \tag{5.24}$$

Or

$$(V_1 - V^-)R_f = (V^- - V_0)R_1 \tag{5.25}$$

$$R_f V_1 - R_f V^- = R_1 V^- - R_1 V_O \tag{5.26}$$

$$-R_f V_1 + (R_f + R_1)V^- = R_1 V_O \tag{5.27}$$

$$V_O = \left(\frac{R_f}{R_1} + 1\right)V^- - \frac{R_f}{R_1}V_1 \tag{5.28}$$

Applying VDR to node b,

$$V^{+} = \frac{R_3}{R_2 + R_3} V_2 \tag{5.29}$$

But. $V^{-} = V^{+}$ Substituting Eq. (5.17) into Eq. (5.16) yield

$$V_O = \left(\frac{R_f}{R_1} + 1 \right) \frac{R_3}{R_2 + R_3} V_2 - \frac{R_f}{R_1} V_1 \tag{5.30}$$

$$V_O = \left(\frac{R_f + R_1}{R_1} \right) \frac{R_3}{R_2 + R_3} V_2 - \frac{R_f}{R_1} V_1 \tag{5.31}$$

$$V_O = \left(\frac{R_f R_3 + R_1 R_3}{R_1 R_2 + R_1 R_3} \right) V_2 - \frac{R_f}{R_1} V_1 \tag{5.32}$$

$$V_O = \frac{R_f R_3}{R_1 R_3} \left(\frac{1 + \frac{R_1}{R_f}}{1 + \frac{R_2}{R_3}} \right) V_2 - \frac{R_f}{R_1} V_1 \tag{5.33}$$

$$V_O = \frac{R_f}{R_1} \left(\frac{1 + \frac{R_1}{R_f}}{1 + \frac{R_2}{R_3}} \right) V_2 - \frac{R_f}{R_1} V_1 \tag{5.34}$$

Since a difference amplifier must reject a signal common to the two inputs, the amplifier must have the property that V_0=0 when**V_1=V_2**. This property exists whe

$$\frac{R_1}{R_f} = \frac{R_2}{R_3} \tag{5.35}$$

Thus, when the Op-Amp circuit is a difference amplifier, Eq. (5.18) becomes

$$V_O = \frac{R_f}{R_1} V_2 - \frac{R_f}{R_1} V_1 = \frac{R_f}{R_1} \left(V_2 - V_1 \right) \tag{5.36}$$

If **R_1=R_f** and **R_2=R_3 ,** the difference amplifier becomes a subtractor, with the output

$$V_O = \left(V_2 - V_1 \right) \tag{5.37}$$

5.5.7 The Integrator Amplifier

An **operational amplifier (Op-Amp) integrator** is a circuit that performs mathematical **integration** of the **input signal**. It produces an output voltage that is proportional to the time integral of the input voltage

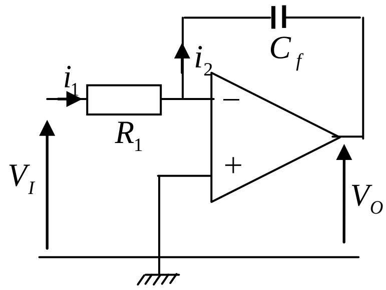


Figure 5-11 : The Integrator Amplifier

The circuit can be analyzed by applying KCL at the inverting input

$$i_1 = i_f \tag{5.38}$$

Furthermore, the capacitor has a voltage-current relationship governed by the equation

$$i_f = C_f \frac{d(V^- - V_O)}{dt} \tag{5.39}$$

Substituting the appropriate variables

$$\frac{V_I - V^-}{R_1} = C_f \frac{d(V^- - V_O)}{dt} \tag{5.40}$$

For an ideal op-amp $V^- = 0\mathbf{V}$, so:

$$\frac{V_I}{R_1} = -C_f \frac{d(V_O)}{dt} \tag{5.41}$$

$$\frac{V_I}{R_1 C_f} = -\frac{d(V_O)}{dt} \tag{5.42}$$

If the initial value of V_O is assumed to be 0 volts, the output voltage wil simply be proportional to the integral of the input voltag

$$V_O = -\frac{1}{RC_f}\int_0^t V_I d(t) \tag{5.43}$$

5.5.8 Op-Amp differentiator

An **op-amp differentiator** (or derivative circuit) produces an output voltage proportional to the rate of change (derivative) of the input voltage. It is commonly used in **signal processing, edge detection, and high-pass filtering**

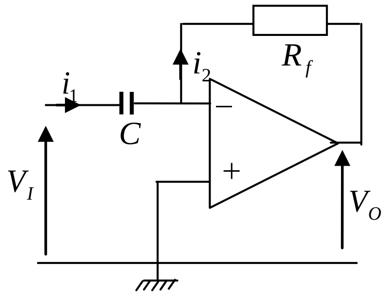


Figure 5-12 : Op-amp differentiator

The circuit can be analyzed by applying KCL at the inverting input

$$i_1 = i_f \quad (5.44)$$

$$i_1 = C\frac{dV_I}{dt} \quad (4.45)$$

$$C\frac{dV_I}{dt} = -\frac{V_O}{R_f} \quad (4.46)$$

$$V_O = -R_f C\frac{dV_I(t)}{dt} \quad (4.47)$$

5.5.9 Op-Amp logarithmic amplifier

An **Op-Amp logarithmic amplifier** (or log amplifier) is a circuit that produces an output voltage proportional to the logarithm of the input voltage. It is useful in applications such as signal compression, signal processing, and nonlinear analog computing.

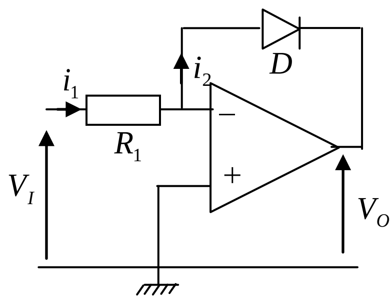


Figure 5-13 : Op-Amp logarithmic amplifier

The circuit can be analyzed by applying KCL at the inverting input

$$i_1 = i_f \tag{5.48}$$

$$i_1 = \frac{V_I}{R_1} \tag{5.49}$$

The following is the **equation for current** flowing through a diode, when it is in forward bias

$$i_f = I_S\left(e^{\frac{U_d}{V_T}} - 1\right) \tag{5.50}$$

$$V_O = -V_D \tag{5.51}$$

$$i_f = I_S\left(e^{\frac{V_O}{V_T}} - 1\right) \tag{5.52}$$

Rearranging this equation gives the output voltage V_O to be aproximately

$$V_O = -V_T \ln\frac{I_f}{I_s} \tag{5.53}$$

$$i_1 = \frac{V_I}{R_1} = i_f \tag{5.54}$$

$$V_O = -V_T \ln\frac{V_I}{R_1 I_s} \tag{5.55}$$

5.5.10 Exponential amplifier

An **anti-logarithmic amplifier** (or exponential amplifier) is a circuit that produces an output voltage that is exponentially related to the input voltage. It is useful in applications like analog computation, signal expansion, and non-linear signal processing.

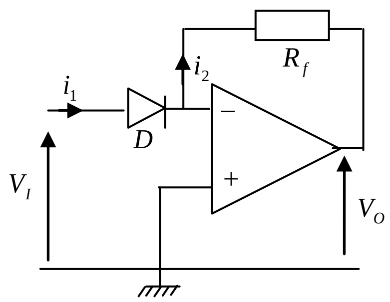


Figure 5-14 : Exponential amplifier

The circuit can be analyzed by applying KCL at the inverting input

$$i_1 = i_f \tag{5.56}$$

$$\frac{V^- - V_O}{R_f} = i_f \tag{5.57}$$

For an ideal op-amp $V^- = V^+ = 0$, so:

$$\frac{-V_O}{R_f} = i_f \tag{5.58}$$

$$i_f = I_S e^{\frac{V_I}{V_T}} \tag{5.59}$$

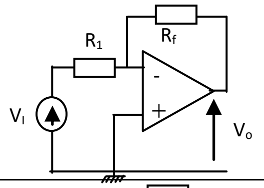
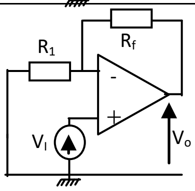
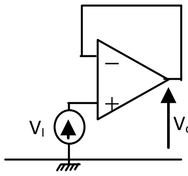
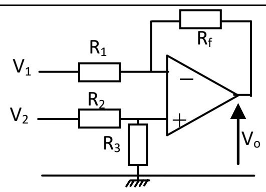
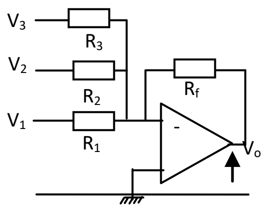
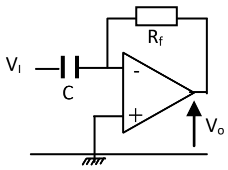
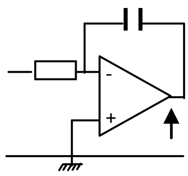
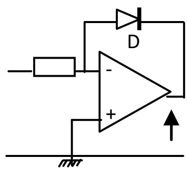
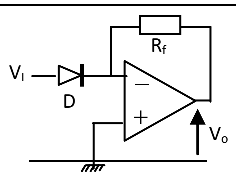
$$-\frac{V_O}{R_f} = I_S e^{\frac{V_I}{V_T}} \tag{5.60}$$

$$V_O = -R_f I_S e^{\frac{V_I}{V_T}} \tag{5.61}$$

5.6 Summary of basic Op-Amp circuits

Table 5-2 summarizes the Op-Amp circuits considered in this chap ter. The expression for the gain of each amplifier circuit holds whether the inputs are DC, AC, or time-varying in general.

Table 5.2 : Summary of basic op amp circuits

Op-Amp circuit	**Name/output-input relationship**
	Inverting Amplifier $V_O = -\frac{R_f}{R_1}V$
	Noninverting Amplifier $V_O = \left(1 + \frac{R_f}{R_1}\right)V_I$
	Voltage follower $V_O = V_I$
	Difference Amplifier $V_O = \frac{R_f}{R_1}(V_2 - V_1)$
	Summing Op-Amp $V_o = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$
	Op-amp differentiator $V_O = -R_f C\frac{dV_i(t)}{dt}$
	Integrator Amplifie $V_O = -\frac{1}{RC_f}\int_0^t V_I d(t)$
	logarithmic amplifier $V_O = -V_T \ln\frac{V_i}{R_1 I_s}$
	Exponential amplifier $V_O = -R_f I_S e^{\frac{V_O}{V_T}}$

5.7 Glossary

Français	**English**	العربية
Amplificateur opérationnel	Operational Amplifiers	المضخم العملي
Domaine de saturation	Saturation region	مجال التشبع
Domaine de linéaire	Linear region	مجال الخطي
Montage amplificateur inverseur	Inverting amplifier	تركيب مضخم عاكس
Monatge amplificateur non inverseur	Nonnverting amplifier	تركيب مضخم غيرمعاكس
Amplificateur suiveur	Voltage follower	مضخم عمليات ملاحق الجهد
Aop additionneur	Summing	مضخم عمليات
Aop intégrateur	Integrator Amplifier	مكامل مضخم عمليات
Aop dérivateur	Derivative circuit	مضخم عمليات مفاضل
Logarithmique	Log amplifier	اللوغاريتمي
Exponentiel	Exponential amplifier	الأسي

OPERATIONL AMPLIFIERS (Op-Amp)

Exercises

Exercise: 05.1

Given the Op-Amp circuit shown in figure 5-15, express

Vo in terms of V_1 and V_2.

a- What does this circuit represent?

$V_1 = 1 + 10\sin\omega t, V_2 = -1V,\ C = 1\mu F, R_1 = R_2 = 100K\Omega$

b- Calculate the value of the output voltage

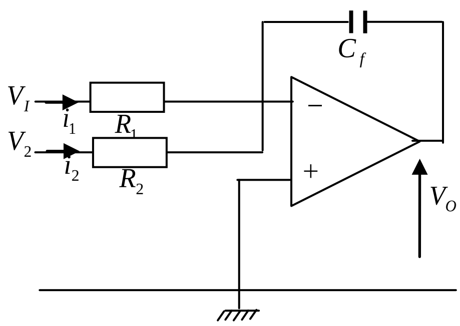


Figure 5-15 : Circuit for Exercise 05.1

Exercise 05.2:

Determine the voltage gain V_O/V_I of the Op-Amp circuit in figure 5-16

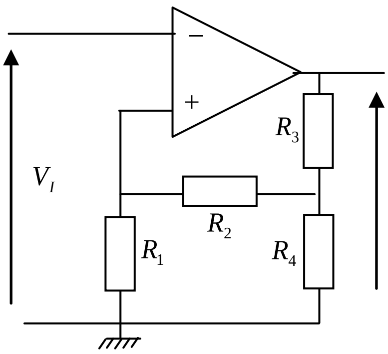


Figure 5-16 : Circuit for Exercise 05.2

Exercise 05.3: Instrumentation amplifier

The circuit in the figure below represents an instrumentation amplifier.

1- What role do the operational amplifiers Op-Amp$_1$ and Op-Amp$_2$ placed at the input of the circuit play?

2- Determine the expression of the output voltage V_O as a function of V_1 and V_2.

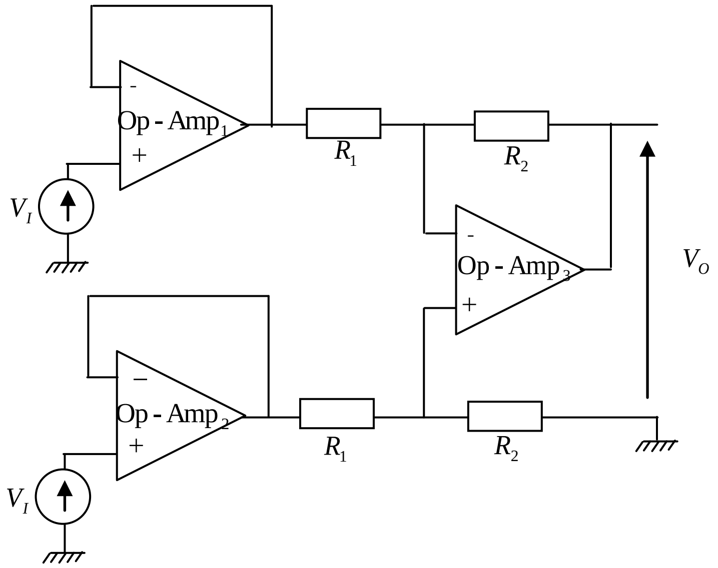


Figure 5-17: Circuit for Exercise 05.3

Exercise 05.4

Considering the circuit in figure 5-18 composed of ideal operational amplifiers, give the expression for the voltage gain

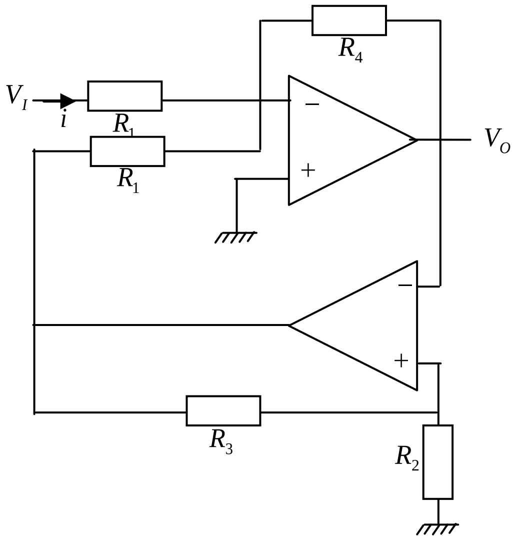


Figure 5-18: Circuit for Exercise 05.4

OPERATIONL AMPLIFIERS (Op-Amp)

Solutions

Exercise 05. 1

a- Operational equations

Application of KCL at the inverting terminal gives (Figure 5-16)

$i = i_1 + i_2$ $\qquad\qquad\qquad V^+ = V^-$

$$V_1 - V^+ = R_1 i_1 \Rightarrow i_1 = \frac{V_1}{R_1}$$

$$V_2 - V^+ = R_2 i_2 \Rightarrow i_2 = \frac{V_2}{R_2}$$

$$V^+ - V_O = \frac{1}{C}\int idt \Rightarrow V_S = -\frac{1}{C}\int idt$$

$$V_O = -\frac{1}{C}\int\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)dt$$

b- The role of the circuit: The circuit represents **an integrator**.

c- the value of the output voltage

$$V_S = -\frac{1}{C}\int\left(\frac{1+10\sin\omega t}{R} - \frac{1}{R}\right)dt = -\frac{10}{CR}\int \sin\omega t dt$$

$$= -\frac{10}{CR\omega}\cos\omega t$$

$$V_S = \cos 100t$$

Exercise 05. 2

Operational equations

$V^+ = V^-$

$i_1 = i_2 + i_3$

$V_I = V_x$

$V_y - V_x = R_2 i_2 \Rightarrow V_y = R_2 i_2 + V_I$

$V_0 = R_3 i_1 + V_y$

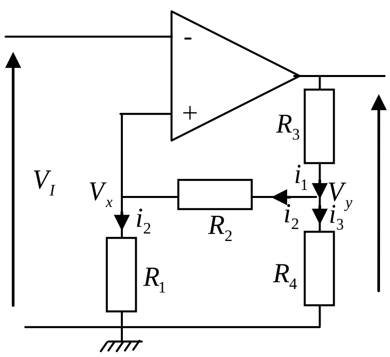


Figure 5-16

$$V_y - 0 = R_4 i_3 \Rightarrow i_3 = \frac{V_y}{R_4}$$

b-**Calculation of the voltage gain**

$$i_1 = i_2 + i_3 = \frac{V_I}{R_1} + \frac{V_y}{R_4}$$

$$i_1 = i_2 + i_3 = \frac{V_I}{R_1} + \frac{R_2 \frac{V_I}{R_1} + V_I}{R_4} = V_I \left(\frac{R_2 + R1}{R_4 R_1} + \frac{1}{R_1} \right)$$

$$V_0 = R_3 V_I \left(\frac{R_2 + R1}{R_4 R_1} + \frac{1}{R_1} \right) + R_2 i_2 + V_I$$

$$V_0 = R_3 V_I \left(\frac{R_2 + R1}{R_4 R_1} + \frac{1}{R_1} \right) + R_2 \frac{V_I}{R_1} + V_I$$

$$V_0 = V_I \left[R_3 \left(\frac{R_2 + R1}{R_4 R_1} + \frac{1}{R_1} \right) + \frac{R_2}{R_1} + 1 \right]$$

$$\frac{V_0}{V_I} = \frac{R_3 R_2}{R_4 R_1} + \frac{R_3}{R_4} + \frac{R_3}{R_1} + \frac{R_2}{R_1} + 1$$

$$\frac{V_0}{V_I} = \frac{R_3 R_2 + R_1 R_3 + R_3 R_4 + R_2 R_4 + R_1 R_4}{R_4 R_1} = \frac{(R_1 + R_2)(R_3 + R_4) + R_3 R_4}{R_4 R_1}$$

Exercise 05. 3

1- role do the operational amplifiers Op-Amp$_1$ and Op-Amp$_2$ placed at the input of the circuit play :

The two operational amplifiers located at the input of the device are configured as voltage followers. In other words, their output voltage is equal to the input voltage applied to the non-inverting terminal. The circuit therefore has an infinite input impedance, both at input V_1 and at input V_2.

2- Determine the expression of the output voltage V_O as a function of V_1 and V_2.

Since no current can enter the third operational amplifier (Figure 5-17), we apply the voltage divider principle at point B, that is, at the non-inverting input of the operational amplifier

$$V_3^+ = \frac{R_2 V_{i2}}{R_1 + R_2}$$

Let us now apply Millman's theorem at point A, that is, at the inverting input of the same operational amplifier

$$V_3^- = \frac{\frac{V_{i1}}{R_1} + \frac{V_O}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}}$$

The output voltage

$$V_1^+ = V_1^- = V_{i1} \Rightarrow V_{i1} = V_{O1}$$

$$V_2^+ = V_2^- = V_{i2} \Rightarrow V_{i2} = V_{O2}$$

One of the two resistors R_2 provides a feedback loop. Therefore, the operational amplifier operates in the linear region

$$V_3^+ = V_3^-$$

$$\frac{\frac{V_{I1}}{R_1} + \frac{V_O}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}} == \frac{R_2 V_{I2}}{R_1 + R_2}$$

$$\frac{\frac{R_2 V_{I1} + R_1 V_O}{R_1 R_2}}{\frac{R_1 + R_2}{R_2 R_1}} == \frac{R_2 V_{I2}}{R_1 + R_2}$$

$$\frac{R_2 V_{I1} + R_1 V_O}{R_1 + R_2} == \frac{R_2 V_{I2}}{R_1 + R_2}$$

$$\frac{R_1 V_O}{R_1 + R_2} == \frac{R_2 V_{I2}}{R_1 + R_2} - \frac{R_2 V_{I1}}{R_1 + R_2}$$

$$V_O == \frac{\frac{R_2 V_{I2}}{R_1 + R_2} - \frac{R_2 V_{I1}}{R_1 + R_2}}{\frac{R_1}{R_1 + R_2}} = \frac{\left(R_2 V_{I2} - R_2 V_{I1}\right)\left(R_1 + R_2\right)}{R_1\left(R_1 + R_2\right)}$$

$$V_s = \frac{R_2}{R_1}\left(V_{I1} - V_{I2}\right)$$

Exercise : 05.4

Operational equations

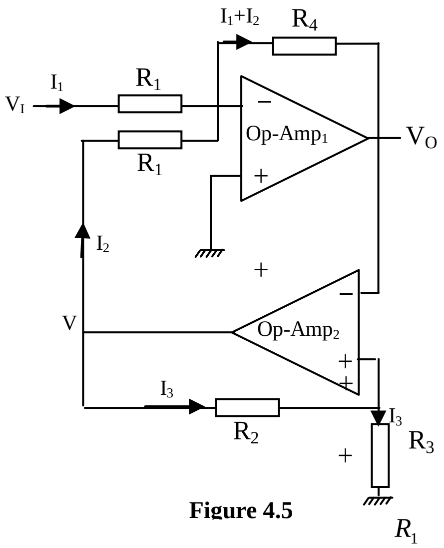


Figure 4.5

$$V_1^+ = V_1^- = 0$$

$$V_2^+ = V_2^- = V_O$$

$$-V_O = R_4(I_1 + I_2)$$

$$V_I = R_1 I_1 \Rightarrow I_1 = \frac{V_I}{R_1}$$

$$V_O - 0 = R_2 I_3 \Rightarrow I_3 = \frac{V_O}{R_2}$$

$$V - V_O = R_3 I_3$$

$$V - V_1^+ = R_1 I_2$$

b-**Calculation of the voltage gain**

$$R_1 I_2 - V_O = R_3 \frac{V_O}{R_2}$$

$$I_2 = \frac{\left(\frac{R_3}{R_2} + 1\right) V_O}{R_1}$$

$$-V_O = R_4 \frac{V_I}{R_1} + \frac{R_4}{R_1}\left(\frac{R_3}{R_2} + 1\right) V_O$$

$$-V_O\left(1 + \frac{R_4}{R_1}\left(\frac{R_3}{R_2} + 1\right)\right) = R_4 \frac{V_I}{R_1}$$

$$\frac{V_O}{V_I} = \frac{-\frac{R_4}{R_1}}{1 + \frac{R_4}{R_1}\left(\frac{R_3}{R_2} + 1\right)}$$

$$\frac{V_O}{V_I} = \frac{-R_4 R_1}{R_4 R_1 + R_4 R_3 + R_4 R_2}$$

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Dr. CHABACHI Salem

Grade : Maître de conférences classe « B »

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Fait le: 20 ماي 2026

Président de CSD

رئيس اللجنة العلمية لقسم
الهندسة الكهربائية
د. أولاد علي عمر

Fait pour valoir ce que le droit